Fabrication of p-n Junction Diode Using Device Fabrication Technology

Pooja Choudhary, Manju Choudhary
Department of Electronics and Communication
Swami Keshvanand Institute of Technology, Management & Gramothan, Jaipur, India
Email: poojachoudhary87@gmail.com

Received 28 February 2017, received in revised form 10 May 2017, accepted 17 May 2017

Abstract: **Diode is the basic semiconductor device which is simply combination of p-n junction. Here p and n junction is positive and negative junction. The p-n junctions are elementary part in the performance of functions such as rectification and switching in circuits. . In this paper, working condition as well as IC fabrication steps are described to fabricate the diodes on silicon wafer. The technology of junction fabrication includes the accumulated knowledge and research for making junctions and forming contact to them in mountings suitable for electronics devices like diode, transistor, FET. Fabrication process depends on materials, processes and methods used to develop highly functional device. . Fabrication of IC is a multistep sequential process like cleaning of wafer, oxidation, etching, diffusion, photolithography and metallization. In this paper, 12,500 diodes are fabricated on 1 inch silicon wafer with resistivity 0.9-1.3 ohm.**

Keywords—VLSI, IC fabrication, wafer, silicon.

1. INTRODUCTION

During 20th century many inventions took place like nuclear power generation, computers, space crafts, mobile phones, etc.

However, everything has to be controlled by electronics. So the invention of Integrated Circuits (IC) by Jack S. Kilby in 1958 is considered to be most important as without ICs the modern communication, space research and all of electronics that are used in this century would have not been possible. Microelectronics technology played a key role in development modern ICs. To-date the dominant semiconductor of microelectronics is silicon as only this material has a natural oxide which is compatible to processes employed in planar technology to fabricate devices and circuits. Above 90% of them are realized in this semiconductor and rest 10%, mostly the opto-electronics belongs to compound semiconductors, mainly GaAs, GaN, InP etc. as it is not possible to make light emitting devices in indirect band gap material Silicon. The discovery of Integrated Circuit there is a race of miniaturization. Miniaturization has been realized to be essential to increase the speed, reduce power consumption, to increase number of transistors on a microchip and more importantly the reliability. The driving force for the miniaturization was Moore's law that states that the component densities on a micro-chip will double every year. To achieve this, the competition for miniaturization led to many inventions in technology and equipments to implement it. The device dimensions keep on decreasing and silicon wafer size keep on increasing. The present scenario is that the 0.10 and 0.08 micron technology is common to fabricate complex ICs and VLSIs, whereas minimum dimensions are few tens of nano-meter and has already been claimed by some fabrication Industries. The wafer size of 8 inch to 12 inch in diameter is also in fabrication line now to enhance the production. Consequently, the modern planar technology has reached to the limit as predicted by Moore's law [1].

1. MATERIALS, CHEMICALS AND EQUIPEMENT REQUIRED FOR THE PROCESS

1. **Wafer:** Silicon wafer of 1 inch diameter, thickness of 400 μm with resistivity 0.9-1.3 ohm and crystal orientation <111> is used for p-n junction fabrication.
2. **Nitrogen and Oxygen gas**: highly pure gases are required with an arrangement of valves and gas flow control.
3. **Bubbler:** for wet gas delivery water bubbler attach with the gas lines is used.
4. **Boron Nitride:** used as P-type dopant.
5. **De-ionized water:** it is required for production of 18Ω resistivity of water.
6. **Chemicals:** necessary electronic grade chemicals are required.
7. **Masks:** required to transfer pattern on silicon wafer.
8. **Ultra sonic vibrator:** required for cleaning purpose.
9. **Vaccum coating unit:** to fix wafer on spinner.
10. **Baking furnace, Mask Aligner & Photoresist Spinner:** used for photolithography.
11. **Voltmeter and Ammeter:** measure characteristics of p-n junction diode.
12. **Others essential items:** microscope, tweezers, Safety Goggles, Covering dress for lab.

3. FABRICATION PROCESS

The advanced technologies of today and tomorrow require monocrystalline Silicon with precise characteristics, oxygen content and controlled dopant. By reducing SiO_2 with Carbon in an electric furnace at a temperature of 1500°C to 2000°C it results in Metallurgical Grade Silicon (MGS) of 98% purity. For bringing impurities below ppb level MGS is further purified. MGS is reacted with HCl to form trichlorosilane (TCS) in a fluidized-bed reactor (300°C) according to the chemical reaction (1)

$$Si + 3HCl \rightarrow SiHCl_3 + H_2 \qquad (1)$$

In this reaction process many impurities such as Al, Fe and B are removed [2]. Obtained TCS is now vaporized, diluted with H2, and flowed into a deposition reactor where it is transformed into Electronic Graded Silicon (EGS) with a purity of 99.99%. This EGS is used for fabrication of ICs. A process used for growing crystal known as C-Z method transforms polycrystalline silicon into a singular crystal orientation, known as ingots. Hence, using various mechanical and chemical process steps turn ingot into a functional wafer [3].

3. VLSI FABRICATION STEPS

(i) Chemical cleaning of silicon wafer

Cleanliness is most important factor in IC fabrication. Circuits are built in ultra clean rooms. Failing to it may cause complete failure of device fabricated.

(a) Glassware cleaning

In approximately 750 ml of DI water put slowly $K_2Cr_2O_7$ or chromium oxide crystal and stir. Add more crystals to make it more saturated. 36 ml of this solution in 1000cc of Sulphuric acid gives cleaning solution for glass wares. Wash beaker in flowing water then immersed it in above solution for few minutes. Beaker is then washed with in water followed by DI water. Beaker is then dried in oven [1].

(b) Silicon wafer cleaning

Silicon wafer is cleaned in order to remove any kind of impurity on it. Wafer is cleaned by using standard RCA process. Dust/grease/oil can be removed by use of Trichloroethylene (TCE), Acetone, and Methanol for 3-5 min followed by Ultra-Sonic agitation. Residual contamination can be eliminated by dipping wafer in 5:1:1::H_2O:NH_4OH:H_2O_2 for 10 min. Native oxides can be removed by dipping in 1:50::HF:H_2O sol. for 10 sec. After each step wafer should be rinsed using DI water [2].

(ii) Oxidation

It is the process by which a layer of silicon dioxide is grown on substrate. During fabrication process accurately controlled thickness of SiO_2 is required. In dry oxidation wafers are heated in dry oxygen ambience oxide quality is good but growth rate is low. During wet oxidation silicon wafer is heated in wet oxygen [3]. Wafer is placed in quartz boat after cleaning as shown in fig.1. Silicon wafer loaded in Quartz boat is gently pushed into middle of pre-heated furnace. Furnace temperature set at a desired temperature of 1050°C.

Oxidation cycle DRY-WET-DRY oxidation cycle is employed arrangement of oxidation process is shown in fig.2 First wafer is subjected to dry oxygen ambient for 20 min. Secondly, water in the oxidation flask is heated to about 80°C-90°C, wet oxygen flow is maintained for about 60 min. after wet oxidation, and dry oxygen is switched on into furnace for 20 min. Wafer boat is pulled out of furnace.

Growth oxide thickness is proportional to temperature of oxidation, water bath temperature and the time of oxidation.

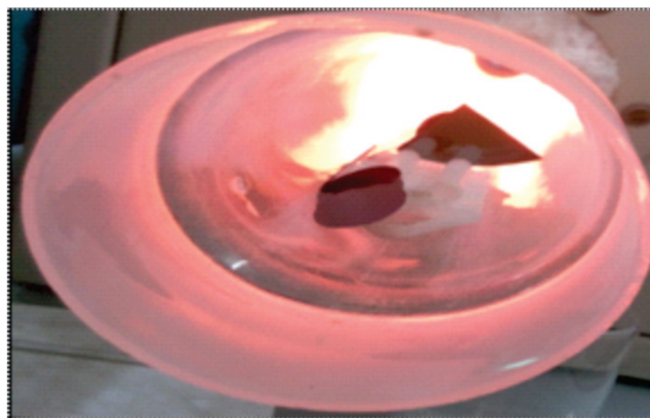

Fig.1 Wafer loaded into furnace for oxidation

Fig.2 Oxidation process arrangement

(iii) Photolithography

Photolithography is an optical means for transferring pattern on to a wafer in the 1:1 ratio. Optical source is used for exposing the wafer through mask [4]. In this process of fabrication positive photo resist is used for lithography.

Steps for Photolithography process as follows:

(a) Photo resist coating using spinning process: wafer is loaded on the spinner using Vacuum arrangement and a few drops of positive photo resist applied. For the formation of

uniform thin layered photo resist (5 μm) the speed of spinner should be maintained at 4000 RPM for better adhesion.

(b) Prebaking: The photo resist is then hardened by baking the wafer in an oven at about 100 OC for 20 min so that photo resist does not run on the wafer surface.

(c) UV Expose: After prebaking, wafer and mask are mounted on mask aligner. Aligner has a precise X-Y and angular arrangement. Printing or transfer of mask pattern on to wafer is done by exposing wafer to UV source for 8 sec with required mask as shown in fig.3.

(d) Development of Photo resist: After UV exposure certain chemical changes occur on selected regions of the wafer.

(e) Post Baking: After resist development the wafer is baked at 120^0C for 20 min to increase the inertness of the resist on the substrate.

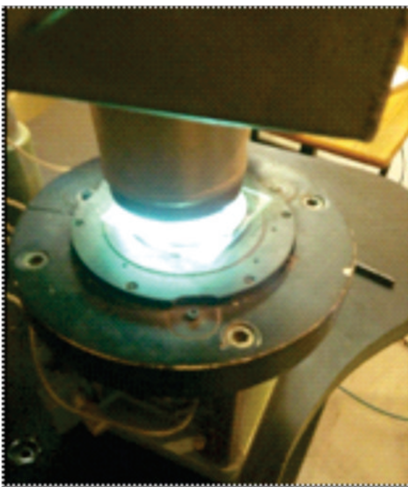

Fig.3 Photolithography process

(iv) Oxide etching

Etching is done to remove SiO_2 which is unprotected by photo resist. The solution used is Buffered Oxide Etch (BOE) (6 parts 40% NH_4F and 1 part 49% HF). These chemicals are handled in plastic beaker wafer is dipped in this solution for 3 min. The SiO_2 layer is completely etched away wafer will appear dry and dull gray.

(v) Diffusion

The process of that introduces atoms of another element into the silicon crystal to alter its conductivity is known as diffusion. Si wafer is n type it is diffused with P type impurity [3].
The diffusion is consists of the following steps:-

(a) Pre deposition of Boron: The silicon wafer and Boron Nitride are placed side by side with a spacing of 2 mm in quartz boat. In the presence of N_2 the boat is gently pushed into the middle of the furnace having a temp of 1000^oC approximately 1 hour. Boron is transported onto the silicon surface and gets deposited as shown in fig.4

(c) Drive in and Borosilicate Glass removal : Due to high temperature impurities are redistributed. In the presence of O_2 gas the furnace is maintained at a temperature of 700^0C. The doped silicon wafer is pushed into the furnace for 10-15 min. The arrangement of diffusion process is shown in fig.5

Due to oxidation and predeposition BSG becomes hard after drive-in Boron glass is removed by dipping wafer in HF solution. Now wafer is ready for metallization [4].

Fig.4 For Diffusion BN with wafer arrangement

Fig.5 Diffusion process placed in boat

(vi) Metallization

The process of depositing thin film of metal is known as metallization. This is done to get metallic contacts and connections. The wafer is placed on the substrate holder as show in fig.6. The vacuum of 5 x 10^{-6} mm of Hg is achieved with the help of rotary (RP) and diffusion pump (DP). Suitable vacuum is required to achieve greater mean free path from source of metal suitable vacuum is required to avoid the collisions with other gas particles. Thermal Evaporation technique is used for metallization [1].

Fig.6 Metallization

(vii) Metal etching

Unwanted metal has to be removed otherwise all diodes will be shorted. Metal etching is shown in fig.7. Soft photo resist is removed via developer. Solution used for metal etching is ortho-phosphoric acid.

Finally a processed wafer is ready for testing.

Fig.7 Metal etching

Characteristics of pn junction diode are measured using voltmeter, ammeter, microscope of 10x. Arrangement of circuit is shown in fig.8.

Fig.8 Circuit arrangement for calculation

Readings of forward bias and reverse bias are shown in table 1.1 and table 1.2.

Table 1.1 Forward bias

Voltage (V)	Current (mA)
0.2	0
0.4	2
0.5	10
0.6	24
0.7	38
0.9	54
1.0	64
1.1	72

Table 1.2 Reverse bias

Voltage (V)	Current (µA)
-10	0
-20	0
-30	0
-35	4
-40	8
-45	18
-50	24
-55	32
-58	80

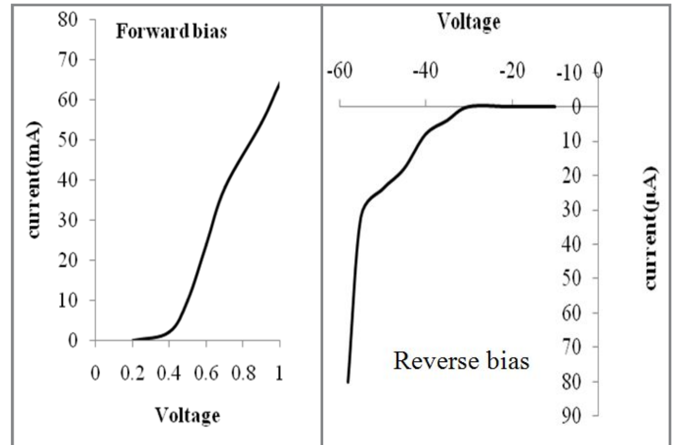

Fig.9 V-I characteristics of diode

Characteristics of diode are plotted on graph between voltage and current as shown in fig.9. 12,500 p-n junction diodes are fabricated on silicon wafer using device fabrication steps.

6. CONCLUSION

We have discussed fabrication steps of practically implemented p-n junction diode. Fabricated p-n junction diode on silicon wafer is shown in fig 1.10. 12,500 diodes are fabricated on a 1 inch circular silicon wafer with resistivity 0.9-1.3 Ω . The cut off voltage is 0.4 V and breakdown voltage is -45 V. V-I characteristics of diode is tested by IV probe method. By analyzing both forward and reverse bias characteristics we came to conclusion that it conducts current only in forward bias.

ACKNOWLEDGMENT

We thank Prof R.P.Gupta (retd.Scientist CEERI-Pilani) who inspired and shared his wisdom with us during this work. He has always provided continuous support, valuable time and immense knowledge.

REFERENCES

[1] Sze, S. M. Semiconductor Devices: Physics and Technology, 2nd ed. New York: John Wiley & Sons, 2002.

[2] Wolf, S., and R. N. Tauker. Silicon Processing for the VLSI Era, 2nd ed. Sunset Beach, CA: Lattice Press, 2000.

[3] P. G. Neudeck, D. J. Larkin, J. A. Powell, L. G. Matus and C. S. Salupo, "2000 V 6H-SiC p-n junction diodes grown by chemical vapor deposition", Appl. Phys. Lett., vol. 64, pp. 1386-1388, 1994.

[4] Stephen Brown and Zvonko Vranesic, “Fundamentals of digital logic design with VHDL design”, 2002.