Performance Analysis of CNFET Based 7T SRAM Cell Using 32nm Technology at Different Supply Voltages

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Abstract: **Carbon Nanotube Field Effect Transistor (CNFET) is known for high performance, stability and low power consumption it is potential candidate to replace silicon in the future. Therefore SRAM Cell design based on CNFET is widely used as low power, highly stable and less delay memory. This paper proposes a new 7T SRAM cell based on CNFET that reduces delay and power consumption during write operation. Read delay and static noise margin are improved by careful cell transistors sizing. In this paper, CNFET based 7T SRAM Cell is designed and its performance analyzed at Vdd 1.8V and 0.9V. HSPICE simulations of the 7T SRAM cell using Stanford CNFET model at 0.9V using 32nm propagation technology shows that power dissipation is reduced by 10.95%, delay is reduced by 0.14%, noise margin at high level is increased by 14.5% and at low level 11.13% , and PDP is reduced by 11.05% in comparison to 7T SRAM Cell at 1.8V.**

Keywords— CNFET, SRAM, HSPICE, Low Power, Power dissipation.

1. INTRODUCTION

VLSI based system and microprocessor require low power as power requirement of portable devices and embedded systems is increasing rapidly. As on chip caches are made up of SRAM Cells and this cache memory is responsible for high speed data transfer between processor and main memory. Conventionally power dissipation composed of read and write power. Write power has higher value than read power due to large power dissipation in driving the cell bit lines to full swing. Various techniques have been developed to decrease the write power consumption by reducing the voltage swing levels on the bit lines. CNTFET was discovered in 1998, since then rapid progress has been done during the past years in all the areas of CNTFET science and technology with inclusion of materials, devices and circuits. As the channel length of device decrease at 32nm then CMOS design and fabrication faces main challenges [1]. In such scenario, CNTFET is a very good choice which has one dimensional band structure with reduction in back scattering and have ballistic transport capability[2]. Good electrical properties of CNTFET such as high speed, high K compatibility and chemical stability have made its performance higher than Si based MOSFET i.e. CMOS. Many studies and researches have been done to analyze the performance of CNTFET at a single device level in the presence of process related non idealities and imperfections at the 32nm technology node using compact CNFET SPICE model [3].

Carbon Nanotube (CNT) can be used as next generation material in VLSI Chip, in particular SRAM Design and it gives solution to problems associated with high integration, performance, stability and low power. The paper is organized as follows: In section II describes the Carbon Nanotube FET, section III introduces the proposed 7T SRAM Cell and its working, section IV contains simulation results and comparisons and section V concludes the paper.

2. CARBON NANOTUBE FIELD EFFECT TRANSISTOR

CNTFET stands for carbon nanotube field effect transistor in which a single carbon nanotube or an array of carbon nanotubes is used between source and drain terminals in the channel region. Here carbon nanotube is the carrier channel and this channel can be controlled i.e. turned on or off by the third terminal (gate) [4]. The layout of CNFET device and relevant parameters based on Stanford CNFET model is illustrated in fig.1

CNT are developed on Si substrate and they are usually straight and parallel in structure. Drain and Source terminals of CNT are heavily doped and they can be any P type or N type transistor. Conventional lithography is used to define the drain, gate and source metal contacts and interconnects. Pitch is the distance between two CNT. Gate width is decided by CNT tube number and pitch [5].

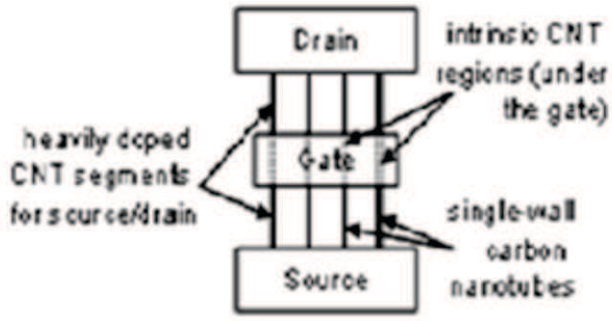

Fig.1 CNTFET Layout

Carbon nanotube can be of two types as single walled carbon nanotube and multi walled nanotube. A single walled carbon nanotube (SWCNT) is made up of single graphene sheet rolled in particular direction[6]. Properties of carbon nanotube whether

it is metallic or semiconducting depends on the chirality vector (m,n) i.e. the direction in that the graphene sheet is rolled[7]. The threshold voltage and diameter of carbon nanotube can be obtained by the following relation as :

$$D = \frac{a}{\pi}\sqrt{n^2+nm+m^2}$$

Where q is the charge of an electron, a=2.49Ao is the CNT atomic distance and Vπ =3.033eV is the carbon π to π bond energy. Size of CNFET depends upon the number of carbon nanotubes. As the mobility of n-type and the mobility of p-type carriers inside CNTs are identical, the minimum size is 1 for both P-CNFET and N-CNFET. Now, CNT can be considered as the most reliable channel material for high performance transistors [8].

3. PROPOSED CNFET BASED 7T SRAM CELL

New proposed architecture of CNFET 7T SRAM Cell is shown in fig.2 [9]. The activity factor denoted as α reduce dynamic power when data is stored in the cell. The proposed 7T SRAM Cell based on CNFET was designed in such a way that it makes read cycle better and decrease the value of dynamic power [8].

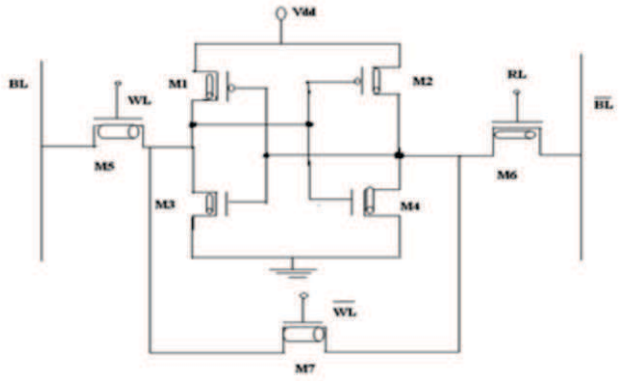

Fig.2 CNFET based 7T SRAM cell

The transistors named as M1, M2, M3 and M4 are arranged in two cross coupled inverters form INV1 and INV2.INV1 and INV2 are arranged in feedback structure such that if low input is applied on INV1 then a high value which is amplified generate on INV2 and vice versa. But this circuit has feedback connection made through an extra NCNFET transistor M7 connection. The node Q and Qbar are used to store data in the circuit[14]. Two transistors named as M5 and M6 respectively are used to write and read data from memory cell. 'Write select' signal is used when data is write into cell. 'Read select 'signal is used when data is read from cell [9].

The proposed 7T SRAM Cell cut off the feedback connection between two inverters INV1 and INV2 when perform the write operation in the circuit. The cut off operation is accomplished by making disconnection through M7 transistor. Hence, M7 is OFF during write operation and M7 is ON during read operation. 'Write bit' is used to perform the write operation in the cell [10].

Read and Write operation:

Read operation is done by applying signal 'Read Select' on M5 and M6 transistor is turned off. Feedback path is connected by applying "Write signal" (W) on the M7 transistor. Now we can read data stored at a node 'Q'. Read cycle can be made better by controlling two aspects as pre charge of the 'Read bit' and size of pull down transistor M4 should be greater than transistor M5 so to get ground path quickly [11].

Write operation is performed by turning off M7 and cut off the feedback connection so that data can be easily stored in the SRAM by applying signal 'Write bit'. The 'Write bit' signal turned on the M6 while M5 is turned off. Two cascaded inverters INV1 and INV2 are formed in 7T SRAM cell.INV1 stores data when 'Write' signal drives M6 and develop QB (Q bar). Similarly, QB develop Q by driving INV2,M3 and M4.After that M6 is turned off again and M7 is turned on to reconnect the feedback path between the inverters to store data easily in the memory cell[12]. Dynamic power value decrease due to reduce switching activity during memory accesses[13]. In 7T SRAM Cell, 'Write bit" does not need to be pre charged for read operation and the write operation is done by affecting single bit line of the cell [14].

4. SIMULATION RESULTS AND COMPARISON

This section contains simulation results of CNFET based 7T SRAM cell at Vdd 0.9V and 1.8V. Simulation results of CNFET based 7T SRAM cell at 1.8V are shown in following figure (3 to 6):

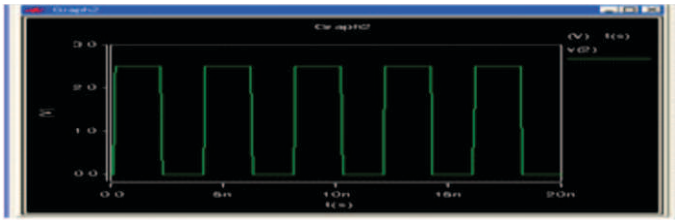

Fig.3 Transient input waveform of CNFET based 7T SRAM cell at 1.8V

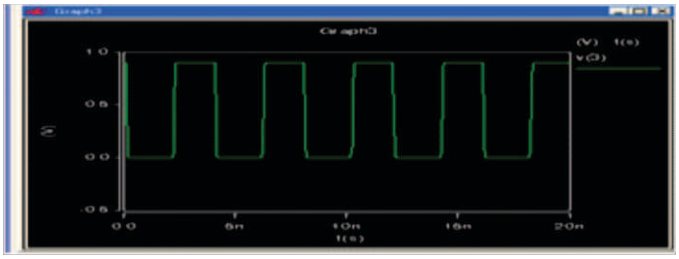

Fig.4 Transient input waveform of CNFET based 7T SRAM cell at 1.8V

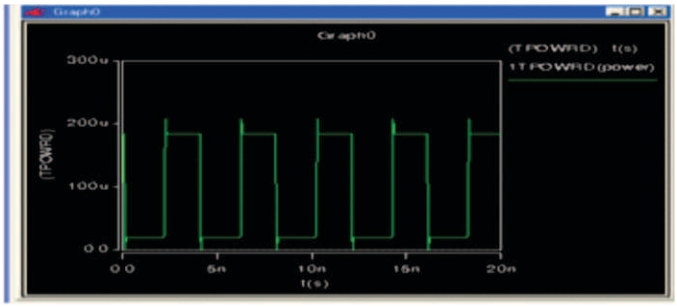

Fig.5 Power dissipated waveform of CNFET based 7T SRAM cell at 1.8V

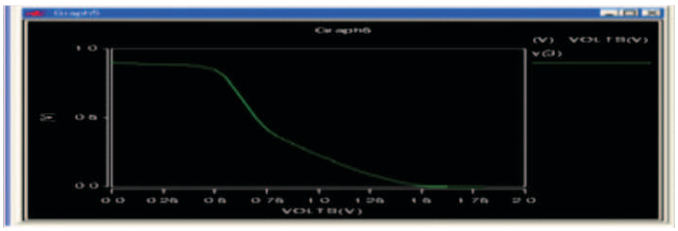

Fig.6 Voltage transfer characteristics of CNFET based 7T SRAM cell at 1.8V

Simulation results of CNFET based 7T SRAM cell at 0.9V are shown in following figure (7 to 10):

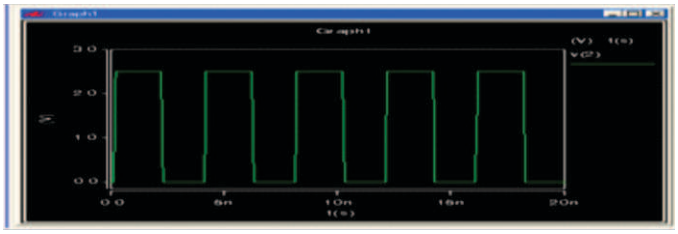

Fig.7 Transient input waveform of CNFET based 7T SRAM cell at 0.9V

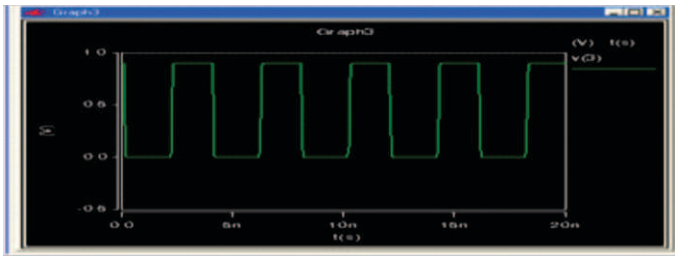

Fig.8 Transient output waveform of CNFET based 7T SRAM cell at 0.9V

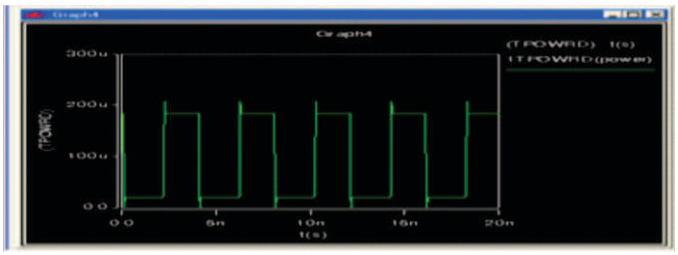

Fig.9 Power dissipated waveform of CNFET based 7T SRAM cell at 0.9V

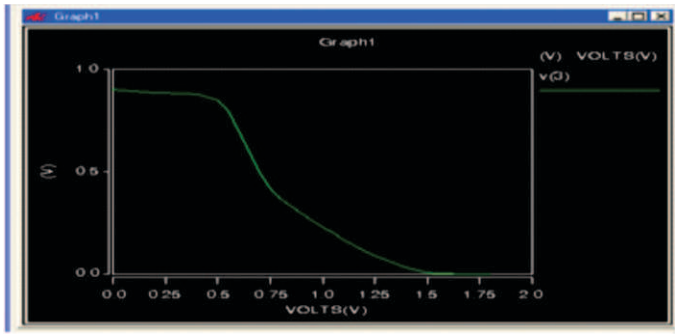

Fig.10 Voltage transfer characteristics of CNFET based 7TSRAM cell at 0.9V

Comparison of simulation results of CNFET 7T SRAM Cell at 1.8V and 0.9V given in following table:

Table : 1 Comparison of Simulation Results

Serial No.	Parameters	CNFET based 7T SRAM cell At 0.9V	CNFET based 7T SRAM cell At 1.8V
1	Noise Margin: NML(in mV) NMH(in mV)	489.1 91.6	440 80
2	Power Dissipated (µ watt)	164.30	184.51
3	Propagation Delay (ps)	20.58	20.61
4	Writing PDP (in Joule)	3.38E-15	3.80E-15

5. CONCLUSION

After comparing CNFET based 7T SRAM cell at Vdd 0.9 and 1.8 V respectively there is increase in low level noise margin by 11.13% and high level noise margin by 14.5% which shows that data stability is highest in 7T SRAM cell at Vdd 0.9V. Power dissipation (10.95%) and PDP (11.04%) less in 7T SRAM cell at Vdd 0.9V it results in low power cache memory and consumes less energy. 7T SRAM cell at 0.9 V is fastest than 7T SRAM cell at Vdd 1.8 V because latter has less propagation delay by 0.14%. After all performance analysis and simulation results it is drawn that CNFET based 7T SRAM Cell at Vdd 0.9V shows best results in terms of noise margin, power dissipation, propagation and power delay product.

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