

# Dstatcom Based Three Phase Four Wire Distribution System For Power Quality Improvement

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**Abstract:** Three phase four wire system is more viable of different power quality problems. In past various methodologies were presented by the researchers to address power quality problems, these problems are namely harmonic distortion, THD levels, load balancing. Recent years the design of Distributed- Static Compensator (D-Statcom) plays an effective role to mitigate load balancing issues. In this paper these problems are taken with a reduced capacity D-Statcom. A zig-zag transformer based D-Statcom is employed to handle power quality issues like poor voltage regulation, compensation of neutral currents and load balancing. This paper presents a Carrier less Hysteresis Control based D-STATCOM to compensate the neutral current in three phase four wire distribution network. Load balancing is also achieved by the controller under different loading conditions. The Simulation studies are performed on MATLAB with Simpower block set.

**Key Words:** Power quality, zig-zag transformer, DSTATCOM.

## 1. INTRODUCTION

Modern power system is very complex and this complexity is increasing with every passing day due to increase in population, heavy industrial load and competitive business environment. Distribution systems are running in stressed conditions due to poor regulation of the power networks. Reliability and quality of power at distribution end is a major issue. However, the effective design of distribution system has many operating constraints namely loss minimization, Power Quality (PQ) improvement, reliability of the power supply etc [1-3].

Due to large variation of electrical loads distribution systems are more vulnerable to the power quality issues. These problems are poor power factor, high neutral current, harmonic current burden and load unbalancing. The source voltage also experiences PQ problems, such as sag, swell, transients, harmonics, flicker and unbalance etc. System load model plays an important role, while observing PQ problems at distribution end. The majority of loads in the distribution system are linear, balanced and unbalanced such as adjustable speed drives in pumps, variable frequency drives and power converters with poor power factor. These loads increase burden on distribution system. Therefore, performance of the distribution system is affected due to reduced power factor, load unbalancing and voltage regulation [4-6]. Many standards were proposed in order to limit the PQ problems such as IEEE Std. 519-1992, IEEE Std. 1159-1995 etc [7-8].

A group of controllers together are called Custom Power Devices (CPDs). CPDs reduce PQ problems of power networks. Distribution Static Compensator (DSTATCOM), Unified Power Quality Conditioner (UPQC), Dynamic Voltage Restorer (DVR), etc. are some of the CPDs devices used to improve the quality of voltage and current in three-phase three-wire & three-phase four-wire distribution systems.

This paper presents application of DSTATCOM to reduce PQ problems in three-phase four-wire distribution network under different operating conditions. DSTATCOM is a shunt connected device, used to compensate the PQ problems at a point of common coupling (PCC). There are various topologies of DSTATCOM are reported in the literature for the correction of PQ problems [9-16]. Some of the topologies of DSTATCOM for 3P4W system for the mitigation of neutral current as well as PQ compensation in the source current which are topology based on Four-leg VSC [14], Three- Single Phase VSC [15], Three-leg VSC with T-connected transformer.[9]. There are various control methodology reported in the literature for the control of shunt active compensators such as power balance theory [10], Synchronous Reference Frame Theory (SRF) [11], Instantaneous Reactive Power Theory (IRPT) [12-15], Symmetrical Components Based Theory (SCBT) [4].

The high neutral currents in three-phase four-wire system have detrimental effect on both distribution system and end users. There are various techniques available to reduce the high neutral current.

In this paper, a new topology of DSTATCOM is planned for a three Phase four Wire distribution systems, which is based on Three-leg VSC with zig-zag transformer. In this technique the zig-zag transformer is connected in parallel to the load for compensating neutral current [3-5]. A zig-zag transformer consists of three single phase transformer with turn ratio 1:1. Therefore the input current flowing into the primary winding is equal to the output current flowing out to the secondary windings. Then three phase currents flowing into three transformers must be identical. Thus the zig-zag transformer can be regarded as open circuit for negative and positive sequence current. Hence the current flowing through the zig-zag transformer is only zero-sequence component.

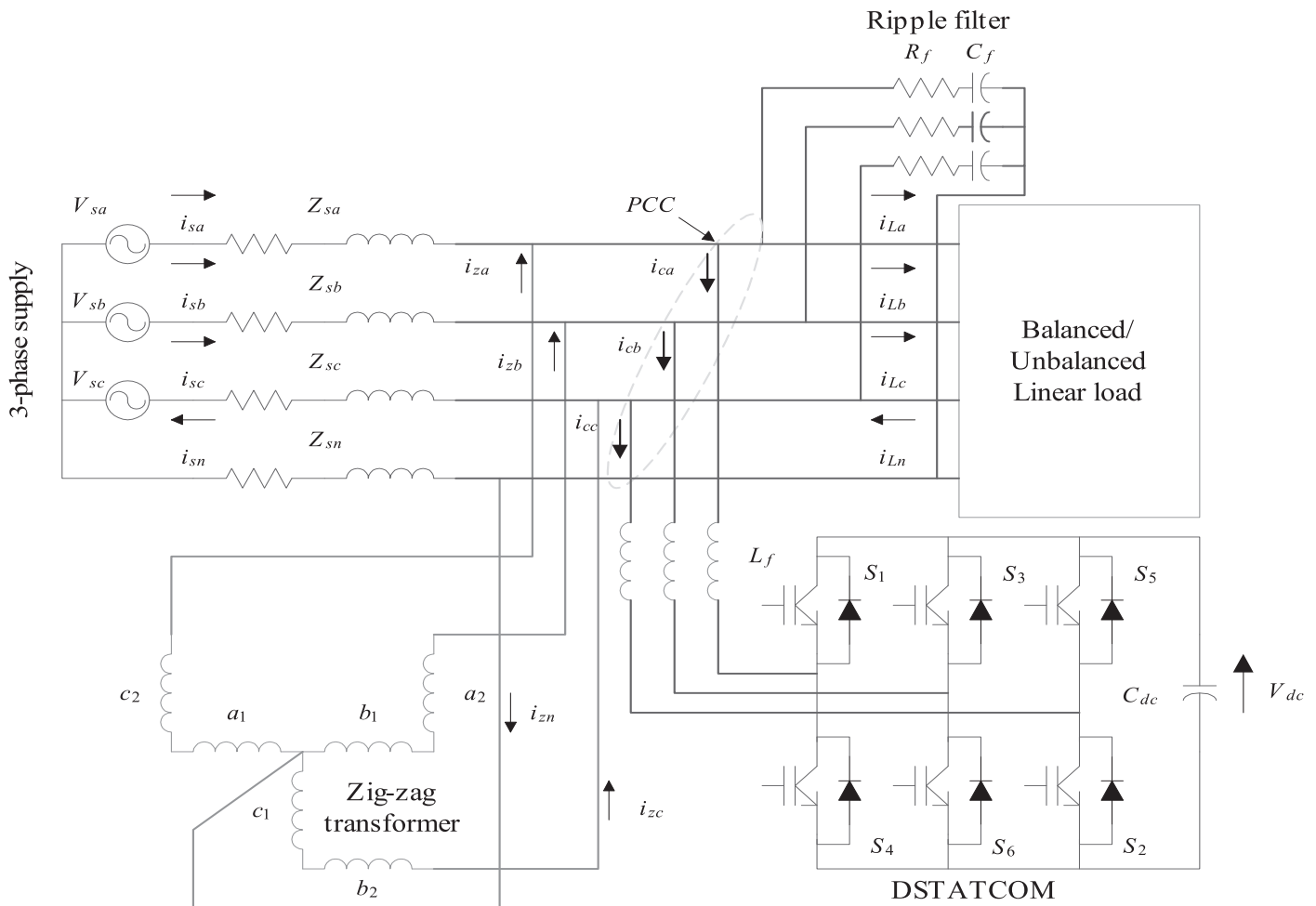


Fig 1: Basic circuit diagram of the DSTATCOM based model

The basic circuit diagram of the proposed methodology is shown in fig.1 [5]. The three phase load may be a lagging/leading loads or combination of all of them. The zig-zag transformer provides a path for the load neutral current. The VSC is realized using six insulated gate bipolar junction transistors (IGBT) switches with anti parallel diodes and a DC capacitor. To reduce the ripples in compensating currents, the interfacing inductors are used to connect the VSC with the supply system. A RC filter is used to filter out the ripples from the supply voltages at PCC [14].

The developed model of DSTATCOM is tested in unity power factor correction (UPFC) as well as zero voltage regulation (ZVR) mode of operation. In PFC mode, the supply voltages and currents are in same phase. In ZVR mode, supply currents are slightly leading the supply voltages [14].

## 2. CONTROL ALGORITHM

The block diagram of the modified control algorithm is based on PI controller based carrier less hysteresis current control which is shown in figure 2 [16]. The PCC supply voltage ( $V_{sa}, V_{sb}$  and  $V_{sc}$ ), supply currents ( $i_a, i_b$  and  $i_c$ ) and dc bus voltage ( $V_{dc}$ ) of the DSTATCOM are sensed as feedback signals to extract the reference supply currents. In this method the unit vectors for in-phase and the quadrature voltages are

obtained from the supply voltage. The in-phase unit vectors ( $u_a, u_b$  and  $u_c$ ) are computed by dividing the ac voltages ( $V_{sa}, V_{sb}$  and  $V_{sc}$ ) by their amplitude  $V_t$ . Another set of vectors called quadrature unit vectors ( $w_a, w_b$  and  $w_c$ ) is a sinusoidal function, obtained from in phase unit vector set ( $u_a, u_b$  and  $u_c$ ). To regulate the PCC terminal voltage, its amplitude  $V_t$  is compared with the desired voltage  $V_{tref}$  and error is processed by means of a PI controller. The PI controller output ( $i_{smq}^*$ ) decides the amplitude of the reactive current to be generated by the DSTATCOM. Multiplication of the quadrature unit vectors ( $w_a, w_b$  and  $w_c$ ) with  $i_{smq}^*$  yields the quadrature component of reference current ( $i_{saq}^*, i_{sbq}^*$  and  $i_{scq}^*$ ).

To provide a self supporting dc bus for the DSTATCOM, the charging current must be provided from the PCC. In order to accomplish this, sensed dc bus voltage ( $V_{dc}$ ) is compared with the dc reference voltage ( $V_{dcref}$ ). The error is processed by means of a second PI controller. The output of PI controller ( $i_{smd}^*$ ) decides amplitude of active power component of the source current. Multiplication of the in-phase vectors ( $u_a, u_b$  and  $u_c$ ) with  $i_{smd}^*$  yields the in-phase component of the reference source currents ( $i_{sad}^*, i_{sbd}^*$  and  $i_{scd}^*$ ). The

reference source currents ( $i_{sa}^*$ ,  $i_{sb}^*$  and  $i_{sc}^*$ ) are obtained by adding the corresponding in-phase and the quadrature components. A pulse width modulation (PWM) current controller then compares the reference source currents ( $i_{sa}^*$ ,  $i_{sb}^*$  and  $i_{sc}^*$ ) with sensed source currents ( $i_{sa}$ ,  $i_{sb}$  and  $i_{sc}$ ) to generate the switching signals for the IGBTs of the DSTATCOM.

The three phase voltages at the PCC ( $V_{sa}$ ,  $V_{sb}$  and  $V_{sc}$ ) are sinusoidal and hence their magnitude is computed as:

$$V_t = \sqrt{\left(\frac{2}{3}\right)(V_{sa}^2 + V_{sb}^2 + V_{sc}^2)} \quad (1)$$

The unit vectors  $u_a$ ,  $u_b$  and  $u_c$  are derived as:

$$\begin{aligned} u_a &= \frac{V_{sa}}{V_t}; \\ u_b &= \frac{V_{sb}}{V_t}; \\ u_c &= \frac{V_{sc}}{V_t}; \end{aligned} \quad (2)$$

The unit vectors in quadrature ( $w_a$ ,  $w_b$ ,  $w_c$ ) are derived from the in-phase unit vectors ( $u_a$ ,  $u_b$ ,  $u_c$ ) using the following transformation.

$$\begin{aligned} w_a &= -\frac{u_b}{\sqrt{3}} + \frac{u_c}{\sqrt{3}}; \\ w_b &= \frac{\sqrt{3}u_a}{2} + \frac{(u_b - u_c)}{2\sqrt{3}}; \\ w_c &= -\frac{\sqrt{3}u_a}{2} + \frac{(u_b - u_c)}{2\sqrt{3}}; \end{aligned} \quad (3)$$

#### A. In-phase component of the reference source current

The dc voltage error  $V_{dcer(n)}$  at the nth sampling instant is  $V_{dcer(n)} = V_{dcref} - V_{dc(n)}$  (4)

where  $V_{dcref}$  is the reference dc voltage and  $V_{dc(n)}$  is the sensed dc bus voltage of the DSTATCOM.

The output of PI controller for maintaining the voltage of dc bus of the DSTATCOM at the nth sampling instant is expressed as.

$$i_{smd(n)}^* = i_{smd(n-1)}^* + k_{pd} \{V_{dcer(n)} - V_{dcer(n-1)}\} + k_{id} V_{dcer(n)} \quad (5)$$

$i_{smd(n)}^*$  is considered as amplitude of active power component of the source current.  $k_{pd}$  and  $k_{id}$  are proportional and integral gain constants of dc bus PI voltage controller, respectively. The in-phase components of reference source currents are estimated as

$$\begin{aligned} i_{sad}^* &= i_{smd}^* u_a; \\ i_{sbd}^* &= i_{smd}^* u_b; \\ i_{scd}^* &= i_{smd}^* u_c; \end{aligned} \quad (6)$$

#### B. Quadrature component of reference source current

The error of ac voltage at the PCC at the nth sampling instant is.

$$V_{er(n)} = V_{tref} - V_{t(n)} \quad (7)$$

Where  $V_{tref}$  is the reference ac terminal voltage of PCC and  $V_{t(n)}$  is amplitude of the sensed three phase ac voltage at PCC at the nth instant. The amplitude  $i_{smq(n)}^*$  of the quadrature component of reference source current at nth instant is derived as output of the PI controller for maintaining ac terminal voltage constant at the nth instant and can be articulated as:

$$i_{smq(n)}^* = i_{smq(n-1)}^* + k_{pq} \{V_{er(n)} - V_{er(n-1)}\} + k_{iq} V_{er(n)} \quad (8)$$

Where,  $k_{pq}$  and  $k_{iq}$  are the proportional and integral gain constant of PI controller,  $V_{er(n)}$  and  $V_{er(n-1)}$  are the error voltage in nth and (n-1)th instant. The quadrature components of the reference source currents are expected as.

$$\begin{aligned} i_{saq}^* &= i_{smq}^* w_a; \\ i_{sbq}^* &= i_{smq}^* w_b; \\ i_{scq}^* &= i_{smq}^* w_c; \end{aligned} \quad (9)$$

#### C. Total reference source current

The whole reference source current is the addition of in-phase and quadrature components of the reference source currents.

$$\begin{aligned} i_{sa}^* &= i_{sad}^* + i_{saq}^*; \\ i_{sb}^* &= i_{sbd}^* + i_{sbq}^*; \\ i_{sc}^* &= i_{scd}^* + i_{scq}^*; \end{aligned} \quad (10)$$

#### D. PWM current controller

In PWM current controller scheme the reference source currents ( $i_{sa}^*$ ,  $i_{sb}^*$  and  $i_{sc}^*$ ) are compared with the sensed source currents ( $i_{sa}$ ,  $i_{sb}$  and  $i_{sc}$ ). The switching patterns of the IGBTs are generated from the PWM current control technique.

The current errors are computed as.

$$\begin{aligned} i_{saerr} &= i_{sa}^* - i_{sa}; \\ i_{sberr} &= i_{sb}^* - i_{sb}; \\ i_{scerr} &= i_{sc}^* - i_{sc}; \end{aligned} \quad (11)$$

These error signals are amplified and then compared with the triangular carrier wave. If the amplified error signal is larger than the triangular carrier wave signal, the lower switch  $S_4$  of VSC is made ON and upper switch  $S_1$  of VSC made OFF. If the amplified error signal is less than the triangular carrier wave signal, the upper switch  $S_1$  made ON and lower switch  $S_4$  made OFF [16].

### 3. RESULT AND DISCUSSION

The performance of the DSTATCOM is tested in power factor correction (PFC) and zero voltage regulation (ZVR) mode of operation.

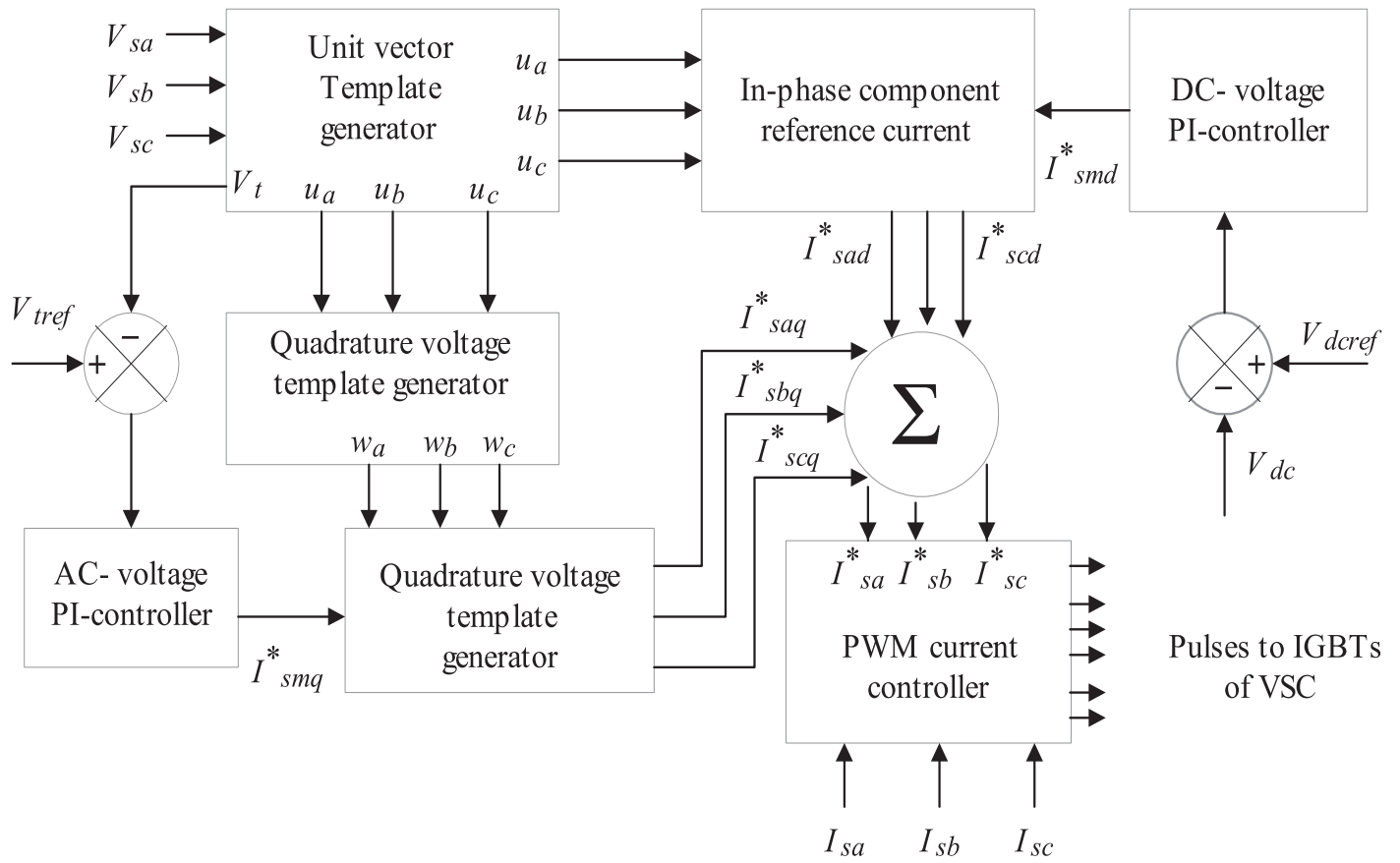
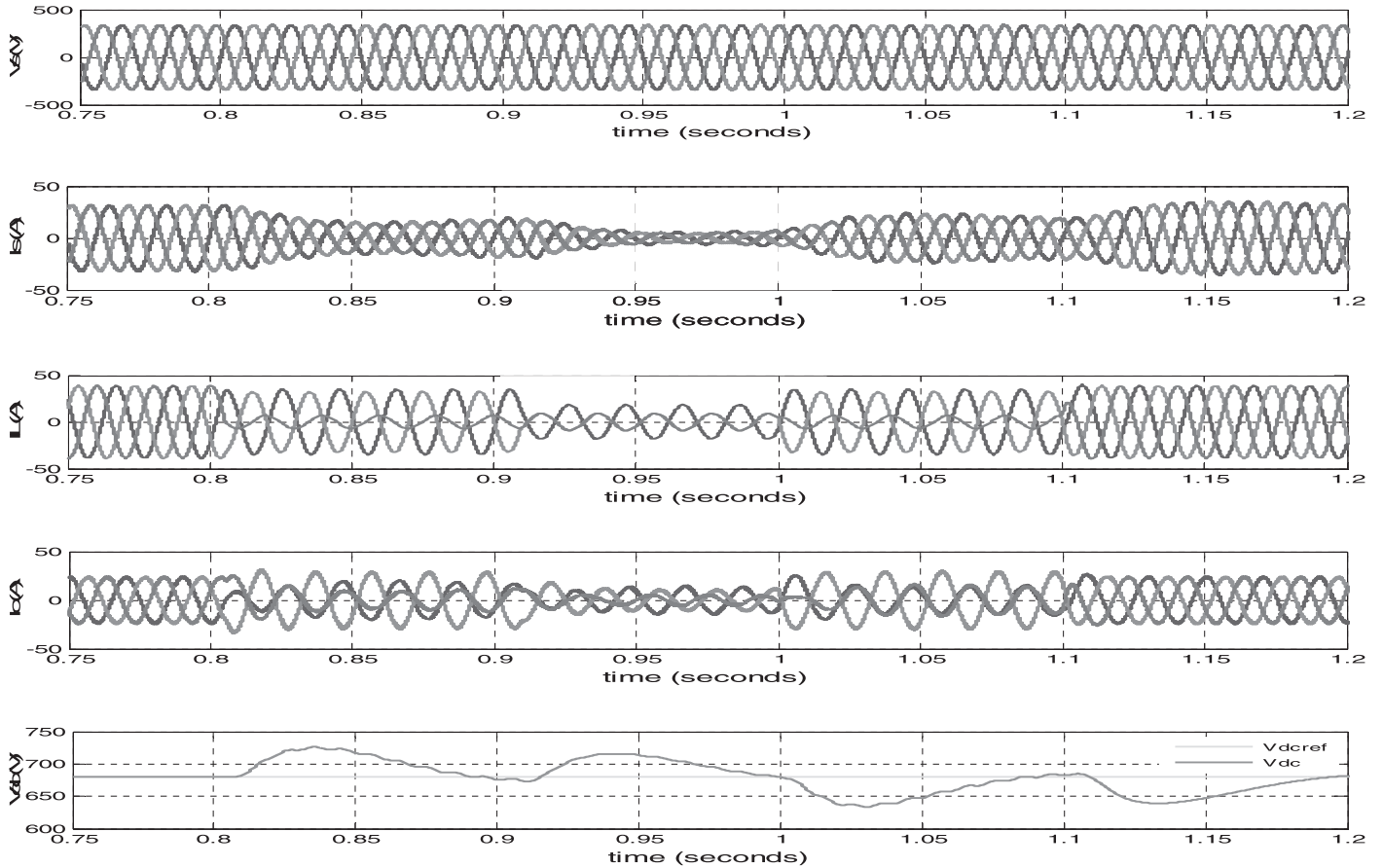


Fig 2: control scheme based on PI controller based carrier less hysteresis current control



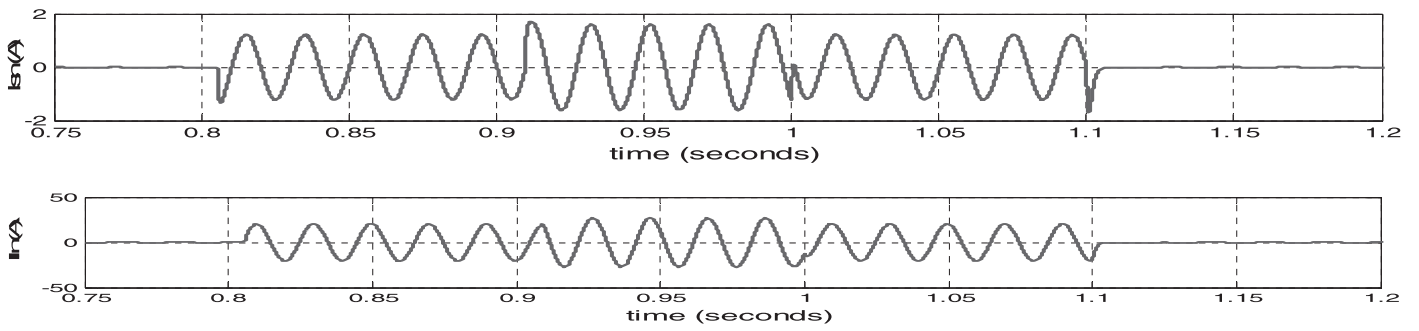


Fig 3: Performance of DSTATCOM with linear load for power factor correction

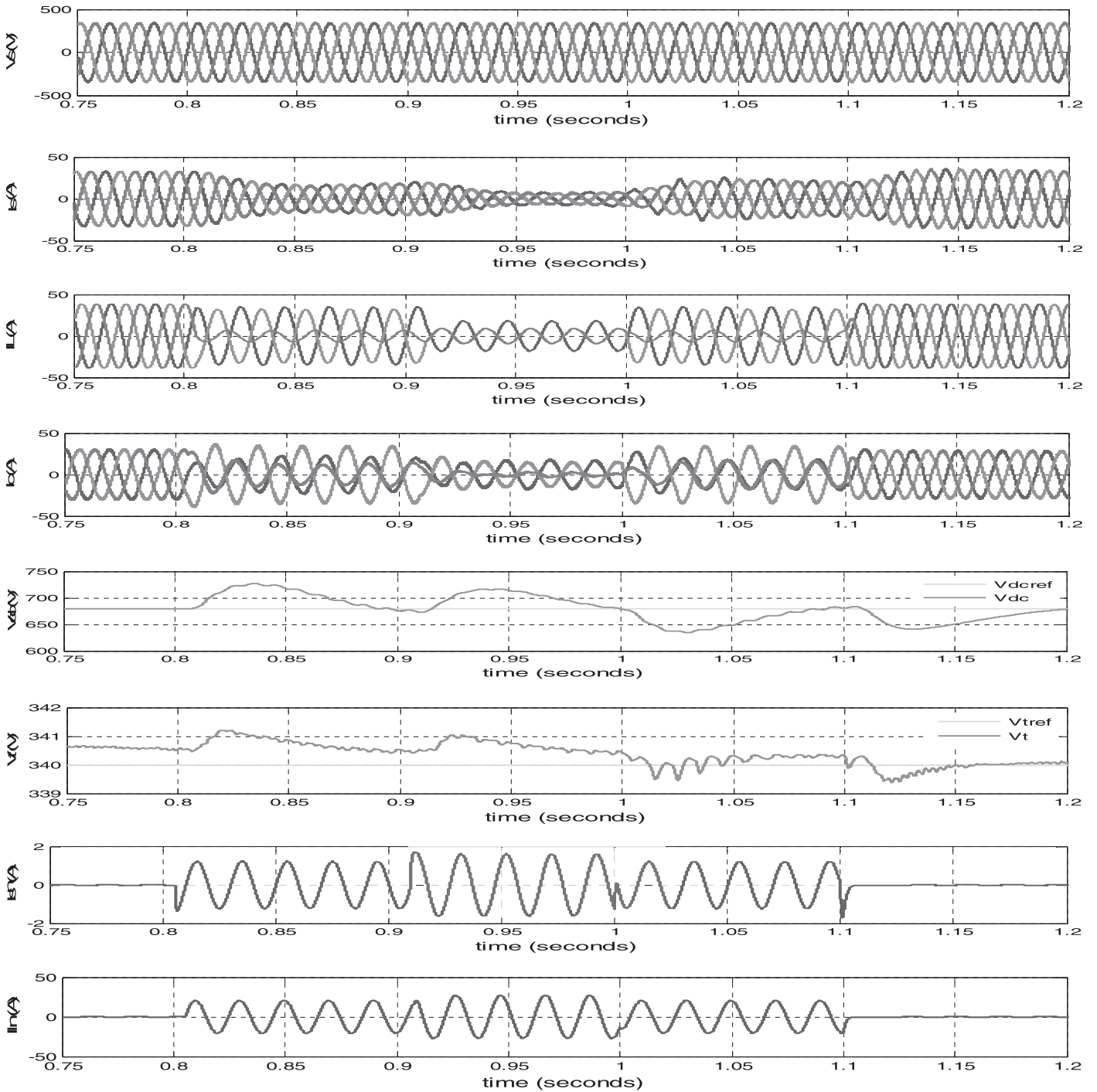


Fig 4: Performance of DSTATCOM with linear load for voltage regulation

### A. Performance of DSTATCOM with zig-zag transformer for three-phase four-wire distribution system

It consists of three single-phase linear loads, zig-zag transformer, DSTATCOM block, ripple filter, CBs, PF, measurements and scope blocks. Initially, the three-phase four-wire distribution system is in stable condition (CB<sub>1</sub> and CB<sub>2</sub> are open). It means that the controller circuit is not connected to the balanced three-phase four wire distribution system. When the CB<sub>1</sub> get closed at 0.8 sec, phase 'c' is disconnected, the resulting load becomes unbalanced. CB<sub>2</sub> get closed at 0.9 sec, phase 'b' is disconnected. CB<sub>1</sub> closed from 0.8 sec to 1.1 sec and CB<sub>2</sub> closed from 0.9 sec to 1.0 sec. Further fault is rectified by controller action. The detail schematic diagram is shown in Figure 1.

#### a. Performance of DSTATCOM in UPF operation mode

Figure 3 show the performance of DSTATCOM for PFC with linear (R-L) lagging load (20 KVA, 0.8 pf). PI controller is use to regulate the DC link voltage to its reference value i.e. 680 V. The performance of variables like source voltages ( $V_s$ ), source currents ( $I_s$ ), load currents ( $I_L$ ), compensator currents ( $I_c$ ), source neutral current ( $I_{sn}$ ), load neutral current ( $I_{Ln}$ ) and neutral current of zig-zag transformer ( $I_{zn}$ ) are shown in Figure 3. It is observed DSTATCOM improve source power factor near unity. The source currents are balanced, sinusoidal and in phase with the voltages. Figure 3 shows phase 'c' is disconnected at  $t = 0.8$  sec & phase 'b' is disconnected at  $t = 0.9$  sec. Again phase 'b' and 'c' are reconnected at  $t = 1.0$  sec and  $t = 1.1$  sec. The source neutral current is reduced by providing the path through a zig-zag transformer & compensates the load neutral current.

#### b. Performance of DSTATCOM in ZVR operation mode

Figure 4 shows the performance of DSTATCOM for AC voltage regulation at PCC with linear (R-L) lagging load (20 KVA, 0.8 pf). The performance of variables like source voltages ( $V_s$ ), terminal voltages at PCC ( $V_t$ ), source currents ( $I_s$ ), load currents ( $I_L$ ), compensating currents ( $I_c$ ), sensed and reference value of DC link voltage ( $V_{dc}$ ) and sensed and reference values of ac terminal voltage ( $V_t$ ), source neutral current ( $I_{sn}$ ), load neutral current ( $I_{Ln}$ ) and neutral current of zig-zag transformer ( $I_{zn}$ ) are shown in Figure 4. Figure 4 shows phase 'c' is disconnected at  $t = 0.8$  sec and phase 'b' is disconnected at  $t = 0.9$  sec. Again phase 'b' and 'c' are reconnected at  $t = 1.0$  sec and at  $t = 1.1$  sec. It is observed from investigation that loads conditions in this mode similar to PFC mode. It is observed that the source currents are sinusoidal, balanced and slightly leading with respect to source voltages. DSTATCOM maintains DC link voltage and AC terminal voltage without any abnormal surge to its reference value i.e. 680 V and 340 V. The source neutral current is also reduced.

## 4. CONCLUSION

The three-leg VSC as a DSTATCOM with zig-zag transformer is modeled and its control has been thoroughly

investigated. The study has been focused towards the development of control scheme that work with simplicity and is easy to implement, offers faster dynamics, robust in operation and have flexibility for future up-gradation. Controller based on carrier less hysteresis current control is presented in this paper. MATLAB simulation reveals that controller is able for load balancing and neutral current compensation. The control algorithm is found more effective to control the DSTATCOM response in PFC & ZVR mode of operation. In PFC mode, power factor is improved. Source currents is balanced, sinusoidal and in phase with voltages. In ZVR mode, load condition is similar to PFC mode. Source currents are balanced, sinusoidal and slightly leading with voltages.

The DC link voltage of DSTATCOM has been found stable in PFC & ZVR mode of operation. AC terminal voltage is also maintained to its reference value. Zig-zag transformer effectively reduced the neutral current. It also enhances the load balancing capability of DSTATCOM.

## 5. APPENDIX

AC line voltage: 415V, 50Hz,  $R_s = 0.01$ ,  $L_s = 1$ mH,

Linear load: 20KVA, 0.08pf,  $R_f = 5\Omega$ ;  $C_f = 5\mu$ F,

DC bus Capacitance: 3000 $\mu$ F,  $V_{dc} = 680$ V.

PWM Switching frequency: 10KHz.

Zig-zag transformer: Three-Single phase transformer of 5KVA, 150/150 V.

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