Recognition of Evolving Faults in Two-Terminal Series Compensated Transmission Line Using DMWT

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Abstract: This paper proposes a discrete Meyer wavelet transform (DMWT)-based evolving faults recognition system for the two-terminal series capacitor compensated transmission line (TTSCCTL). The particular region captured currents of the TTSCCTL are used to estimate the DMWT outputs. To authorize the performance of the DMWT, simulation studies have been done thus varying fault type, resistance, and switching time. The main advantage of DMWT is that it correctly recognizes all types of evolving faults in TTSCCTL by employing one-side fault current data only. It is also investigated that the proposed technique is robust to the deviation in the input fault parameters of TTSCCTL.

Keywords: Evolving faults, fault recognition, TTSCCTL.

1. INTRODUCTION

Among the different components of power transmission and distribution system, protection of transmission lines is very obligatory because the transmission lines are the most expected to experience faults. Detection of fault in transmission lines is essential to provide adept and regular power flow. Many researchers proposed techniques for TL faults recognition and categorization. In recent times, the relevance of wavelet transform has been effectively tested by many researchers for the TL protection. Capacitive compensation of TL by using series capacitors not only balance the XL of TL but also enhances the competence of power transfer of line.

Several works addressed the subject related to fault recognition and categorization in TTSCCTL's. A few important research works are presented in concise here. In [1], finite-state machine-based technique has been used for the protection of transmission line. In [2], variational mode decomposition has been used for detecting faults in transmission line. In [3], DWT (discrete wavelet transform) and SVM (support vector machine) have been utilized for fault detection and classification in transmission line. K-nearest neighbour has been used for parallel TLs [4]. Further, the fault is detected on a TL using EMD and RBDT [5]. In [6], data-mining and mathematical morphology-based technique has been proposed for the detection of high impedance faults in transmission line. In [7], the fault is classified using alienation technique. In [8], artificial neural network has been employed for fault detection and classification. Wavelet transform has been used for fault detection during power swing in [9]. In [10], a differential power protection technique has been proposed for the UPFC connected DCTL.

In this work, DMWT is used for the recognition of evolving faults in TTSCCTL. The authors have not seen this type of work so far. The outcomes prove that the DMWT-based proposed technique expertly recognizes the evolving faults.

This manuscript is prepared like: The description of TTSCCTL is detailed in section-2. The DMWT-based fault recognition technique is detailed in section-3. The outcomes are detailed in section-4 and section-5 ends the paper.

2. DESCRIPTION OF TTSCCTL

The planned DMWT-based process is executed on a 400 kV three-phase, 50 Hz series capacitor compensated transmission line of length 200 km [11]-[12]. Fig. 1 exemplifies the schematic of proposed network. At both the terminals of a transmission line, a 400 kV power source is connected. The TTSCCTL is separated into two parts each having 100 km length. The current measuring devices are installed at bus-1 (relaying point) of a TTSCCTL. To realize the simulation studies, this 400 kV TTSCCTL has been designed and simulated for various types of faults using MATLAB software. For each and every fault case, the fault factors are varied in order to investigate the impact of varying the fault factors on the performance of DMWT-based fault recognition technique.

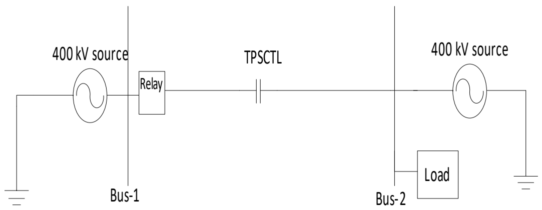

Figure 1: The schematic of 400 kV TTSCCTL

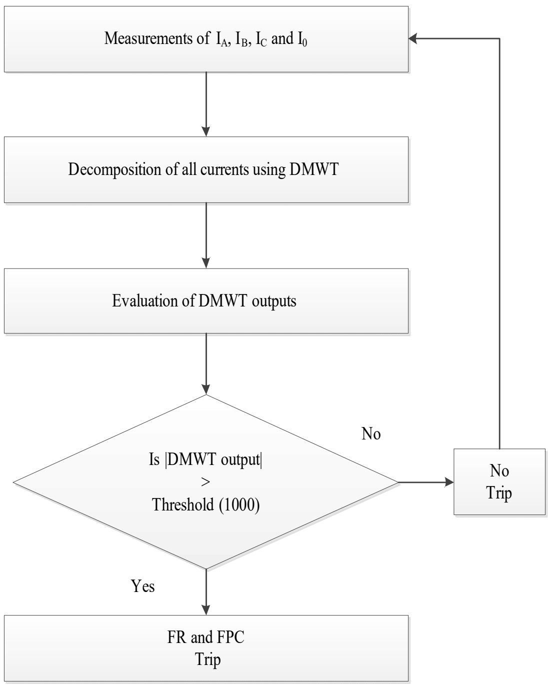

Figure 2: The procedure of fault detection using DMWT

3. DMWT-BASED EVOLVING FAULTS RECOGNITION TECHNIQUE

The DMWT is used in this work because it is a 2D signal processing/filtering tool. It can be used for the processing/filtering of the 2D fault signals. The DMWT extracts the features of the current signals during the filtering process.

In this work, the DMWT is utilized because it decomposes the fault currents into approximate and detail outputs at different decomposition levels and has many advantages over the other fault detection tools. Fig. 2 details the DMWT-based proposed fault recognition technique [13]-[15]. The steps are shown beneath.

- **Step 1** Run the TTSCCTL for various fault types. Measure IA, IB, IC and I0.
- **Step 2** Apply the DMWT on IA, IB, IC and I0 and calculate the outputs of DMWT.
- **Step 3** Select a common threshold value for all the cases of faults by doing different types of simulation studies. In this work, a common threshold value of 1000 is selected after carrying out extensive simulation studies.
- **Step 4** The phase will be proclaimed as the faulted phase and the relay will issues the trip signal when DMWT output of three-phase currents exceeds the threshold value, else there will be no-fault in TTSCCTL.

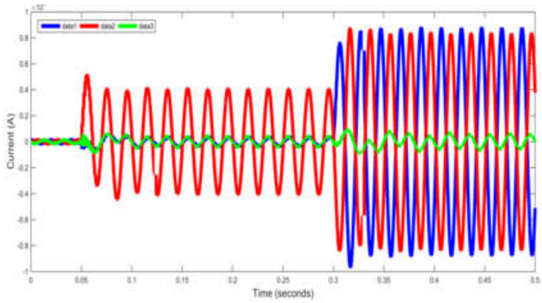

Figure 3: The waveform when BG fault is evolved into ABG fault

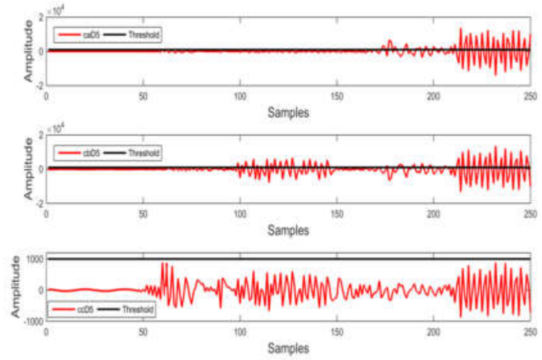

Figure 4: DMWT output when BG fault is evolved into ABG fault

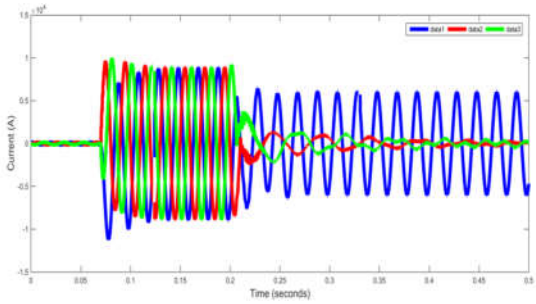

Figure 5: The waveform when ABCG fault is evolved into AG fault

4. OUTCOMES AND DISCUSSIONS

The DMWT is tested for different types of evolving faults among variation in the fault factors such as fault resistance (RF), fault switching time (FST), and location of fault (FL). The outcomes of the proposed work are presented below in different subsections.

4.1. The Efficacy of DMWT for Evolving Faults

The potential of DMWT-based scheme has been tested for various types of evolving faults [16]. An evolving fault is a type of fault wherein one fault type at a particular time is evolved into another fault type at some different time. Numerous simulations have been done to test the effect of evolving faults on the ability of DMWT-based scheme. Fig. 3 depicts the currents, and the DMWT outputs are presented in Fig. 4. Initially, BG fault has been simulated at 0.05 s among FR = 5 Ω and GR = 0.01 Ω at 100 km. This BG fault after few cycles of current waveform is evolved into ABG fault at 0.3 s among FR = 10 Ω and GR = 0.01 Ω. The fault inputs selected are: FL = 100 km and GR = 0.01 Ω. The values of fault resistance, time, and fault location are varied throughout the simulation studies of evolving faults. The switching time difference of both the faults is 0.25 seconds.

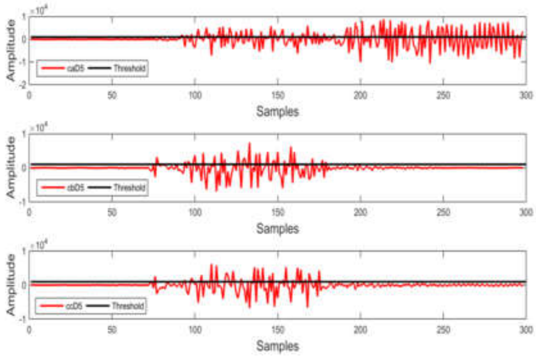

Figure 6: DMWT output when ABCG fault is evolved into AG fault

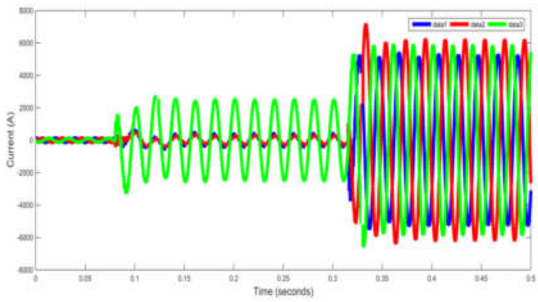

Figure 7: The waveform when CG fault is evolved into ABCG fault

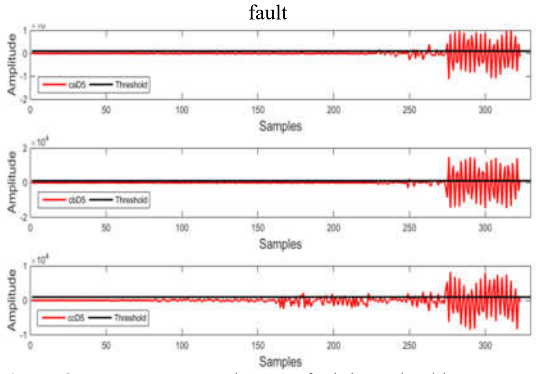

Figure 8: DMWT output when CG fault is evolved into ABCG fault

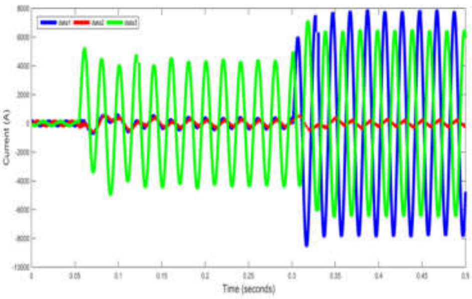

Figure 9: The waveform when CG fault is evolved into ACG fault

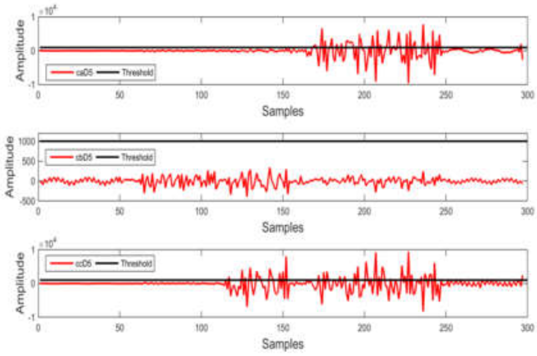

Figure 10: DMWT output when CG fault is evolved into ACG fault

In Fig. 4, it is clearly seen that the DMWT outputs of faulty phases A and B are above the threshold after FST while that of phase C are below the threshold. Figures 5-12 depicts the simulation outcomes for various evolving faults. Fig. 5 shows the waveform when ABCG fault is evolved into AG fault and Fig. 6 depicts its DMWT output. Fig. 7 shows the waveform when CG fault is evolved into ABCG fault and its DMWT output is presented in Fig. 8. Fig. 9 illustrates the waveform when CG fault is evolved into ACG fault and its DMWT output is illustrated in Fig. 10. Fig. 11 represents the waveform when BG fault is evolved into CG fault and its DMWT output is depicted in Fig. 12. Table 1 details the outcomes of the DMWT for different evolving faults. The simulation outcomes as detailed in Table 1 authenticate the competence of DMWT for the recognition of evolving faults as well. Also the proposed scheme perfectly discriminates between the faulty and the healthy phase as well. From Table 1, it is recognized that the evolving faults not affects the performance of DMWT-based proposed technique.

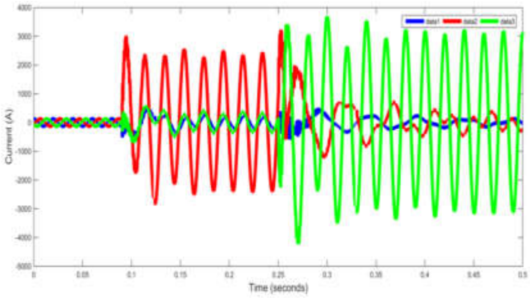

Figure 11: The waveform when BG fault is evolved into CG fault

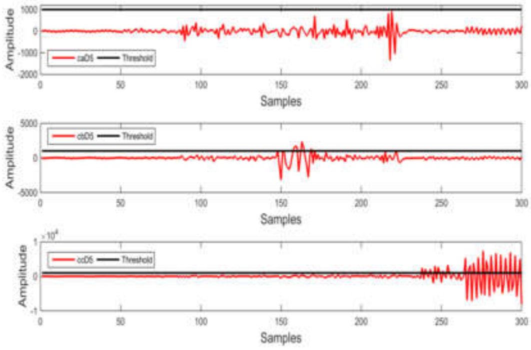

Figure 12: DMWT output when BG fault is evolved into CG fault

5. CONCLUSION

In this paper, a DMWT-based evolving faults recognition technique for a two-terminal series capacitor compensated transmission line (TTSCCTL) has been presented. Broad study of simulations has been investigated including fault type, location, resistance, and switching time deviations. Moreover, it is observed that all the above mentioned fault inputs do not concern the response of DMWT. Simulation outcomes verify the power of DMWT for recognition of evolving faults in TTSCCTL.

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