Design and performance analysis of A Triple Material Double Gate Cylindrical Gate All Around (TMDG CGAA) MOSFET in Nano-meter Regime

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Abstract :The current work deals with the designing and performance analysis of a Triple Material Double Gate Cylindrical Gate All Around (TMDG-CGAA) MOSFET in the nanometer regime. The proposed structure has combined the gate engineering technique by used a double gate structure and the material engineering techniques by used three different materials in the gate electrode to incorporate the benefits of both the techniques. The proposed structure has been verified by using the ATLAS tool, which is a 3-dimensional tool. A comparative study of SG-CGAA, DG-CGAA, DMDG-CGAA, and TMDG-CGAA has been accomplished by using the same device parameters. The threshold voltage (Vth) is extracted from the transfer characteristic of the above MOSFETs. Along with the threshold voltage extraction the other parameters like DIBL and I_{on}/I_{off} ratio are also calculated. Results disclosed that the TMDG-CGAA MOSFET gives better immunity to the SCEs like DIBL. Also, the ratio of on current is to off current is also high in the TMDG-CGAA MOSFET in comparison to SG CGAA MOSFET and DGDM-CGAA MOSFET structures. In the short channel planar devices, the potential barrier is reducing so that the threshold voltage is also reducing. But in the proposed structure the device shows better performance, it increases gate controllability and reducing the SCEs and increment in the high drain current along with the high packaging density, which is needed in the application of Ultra Large Scale Integration (ULSI).

Keywords–TMDG CGAA MOSET, DIBL, Threshold voltage, SCEs.

5. INTRODUCTION

To give superior exemption to SCEs in the nanometer regime the MOSFET can be improved from conventional MOSFETs to Cylindrical Gate All Around (CGAA) MOSFETs. Many structures with multiple gates i.e., double-gate MOSFET, triple gate MOSFET, quadruple gate MOSFET, and cylindrical gate all around MOSFET have been invented to reduce the SCEs [1-4]. Although the multigate devices show better immunity to SCEs and device performance the drain current reduces in these multiple gate structures. Gate electrode is covered around the channel in the GAA devices, which enhances gate controllability. And also enhances current.

In the CGAA MOSFETs, due to the cylindrical structure, the current drive per unit Silicon area gives the great electric field incarceration. As the electric field at the Si/Sio_2 involvement enhances that's why the off current does not enhances the cylindrical gate structures [5]. So the enhanced on current and reduced off current provides the better I_{on}/I_{off} ratio. The proposed TMDG-CGAA structure is the cylindrical version of the TMDG planar MOSFET. In the proposed structure, both gate engineering and material engineering are combined for achieving both technique's benefits. The double-gate MOSFET structure rises the volume inversion so the electrical characteristics I_{on}/I_{off} ratio increases [6]. This results that the double gate structures are more efficient in gate controlling.

As the gate voltage controllability decreases on the drain current, there will be sub-threshold conduction in the transistor. Because when the channel length of MOSFET keeps short the top sideways electric field drifts velocities of majority carriers saturate. Three dissimilar materials with three dissimilar work functions are used for the gate in the proposed work. The largest value of work-function is placed near to source terminal so that the carriers can accelerate more rapidly in the channel region and the smallest value of work-function is placed near to drain terminal so that the electric field peak can be reduced at the drain terminal so the Hot Carrier Effect (HCE) for the n-channel MOSFETs (for p-channel vice versa) also reducing [7].

The proposed structure has superior gate controlling because of the cylindrical structure with the double gate and also decreased the SCEs and improves the drain current due to the triple material used in both the gates. Also, the comparison is done in CGAA, DG-CGAA, and TMDG-CGAA. The simulation is done by the ATLAS 3D device simulator.

Gate electrode controls the channel region in the long channel device MOSFET. Source and drain terminal controls the gate electrode in the short channel device instead of the channel region in the short channel length devices. Some negative and worse effects occur due to the short channel. In the short channel length devices. A device having the channel length is of the similar order of magnitude when depletion-layer widths (x_{dD} ,x_{dS}) of the drain and source terminal, this is known as a short channel device. Because of this short channel, short channel effects (SCE) came into light.

When the channel length is shortened the device suffers from the SCEs. By this SCEs the device starts behaving differently from the long channel device. These SCEs affect device performance, reliability, and mobility. There are many Short Channel Effects like Hot carrier effects, DIBL, a threshold voltage (V_{th}) roll-off, etc [8-10].

6. DEVICE STRUCTURE

Fig.1. shows the 3D simulated structure of a Triple Material Double Gate-Cylindrical Gate All Around (TMDG-CGAA) MOSFET structure by 3D ATLAS tool. Two gates are used in this structure to control the current and reduce the short channel effects. Tube shaped channel is controlled by the internal gate and the external gate in this structure.

The internal gate is used to increase the charge control in the channel region because the internal gate is covered by the oxide layer. And the external gate has similarities to the Gate All Around devices. The internal gate and the external gate have three dissimilar materials and work functions. These three materials are arranged from source to drain is: Aurum Au (ϕ_{m1} = 4.8eV), Molybdenum Mo (ϕ_{m2} = 4.6eV), Titanium Ti (ϕ_{m3} = 4.4eV). The ratio of the channel length L_1:L_2: L_3 is 1:1:1. The channel region of the device is lightly doped with the acceptor concentration (N_A = 10^{18} cm^{-3}) and the source and drain regions are highly doped with the donor concentration (N_D = 2× 10^{20} cm^{-3}). The SiO_2 is used as the gate oxide with the dielectric constant equal to 3.9. The horizontal and radial direction of the channel is taken on the z-axis and radius. Analysis of the following device characteristics of the designed MOSFET is done using the ATLAS tool, which is a 3D device simulator from SILVACO Inc.

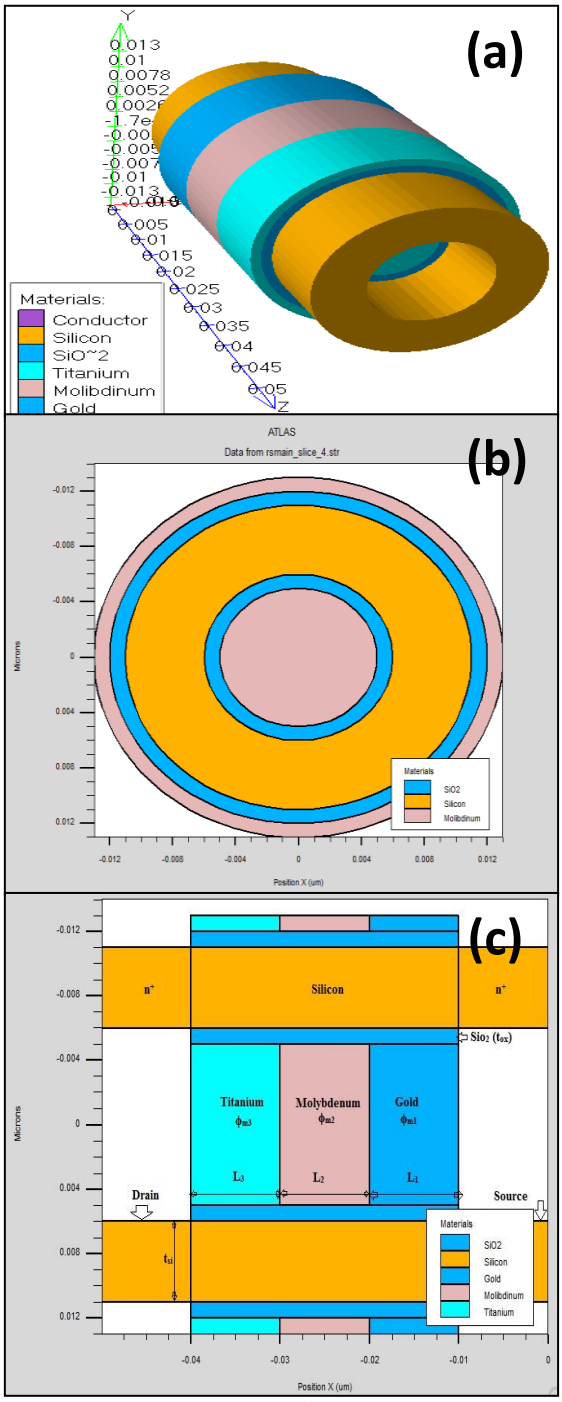

Figure 1 3D simulated structure of TMDG-CGAA MOSFET of 30nm channel length (a) Simulated structure of TMDG-CGAA MOSFET (b) 2D cross-sectional view of TMDG-CGAA MOSFET (c) Cross-sectional view along the channel length

In fig 1 (c) horizontal x-axis is used for z-direction and the vertical y-axis is used as a radial direction. Work functions are arranged in a manner that the highest work-function material Au (Aurum) is placed near to the source and the lowest work-function material Ti (Titanium) is kept near the drain terminal. The L1, L2, and L3 are channel lengths under material M1, M2, and M3

respectively. Design parameters of the TMDG-CGAA MOSFET are listed below in Table I. All the parameters are taken the same for comparison of CGAA, DG-CGAA, and TMDG-CGAA MOSFET at the same channel length 30 nm.

Table I indicates the design parameters for the TMDG-CGAA MOSFET. Si thickness is taken as 5nm for all the CGAA design structures. The gate oxide thickness (t_{ox}) is 1nm. The Sio_2 is used as the gate oxide with the dielectric constant equal to 3.9.

Table 1. List of design parameters of TMDG -CGAA MOSFET

Parameters	Symbols	Values
Oxides thickness	t_{ox}	1nm
Doping Concentration of channel	N_A	1×10^{18} cm^{-3}
Doping Concentration of Source and Drain	N_D	2×10^{20} cm^{-3}
Aurum (Au) work function	ϕ_{m1}	4. 8eV
Molybdenum work function (Mo)	ϕ_{m2}	4. 6eV
Titanium Work function (Ti)	ϕ_{m3}	4. 4eV
Combined Channel Length	L_G	30 nm
Metal Channel Length M1, M2 and M3	L_{G1}, L_{G2} & L_{G3}	10 nm
Channel thickness	tsi	5 nm
Core Radius	R	5 nm
Length of Source/Drain	L_S/L_D	10 nm

7. RESULTS AND DISCUSSIONS

The transfer characteristics (I_d-V_g) of single gate CGAA MOSFET and DG-CGAA MOSFET at channel length (L_g = 30 nm) is compared in the below fig 2. Design parameters are taken the same to compare both the designs SG CGAA MOSFET and DG CGAA MOSFET. I_d-V_g characteristics are plotted at constant voltage V_{DS} = 1V the gate voltage (V_{gs}) is varying from 0 v to 1 v.

By analyzing the fig.2, it can be stated that in the DG-CGAA MOSFET decreased the threshold voltage roll-off than the SG-CGAA MOSFET. The gate to source voltage is changing between the 0V to 1V and at the V_{DS} = 1V, the maximum drain current (I_D) is 0.1628 mA and 0.3052 mA for SG-CGAA MOSFET and DG-CGAA MOSFET respectively. In the double gate structure the value of the drain current increases due to both inner gate and outer gate[11-17]. The channel region is controlled by both the gates, so the drain current enhances, so the on current enhances, and also the off current reduces. Thus the I_{on}/I_{off} ratio is effectively increased in the DG CGAA MOSFET than the SG CGAA MOSFET.

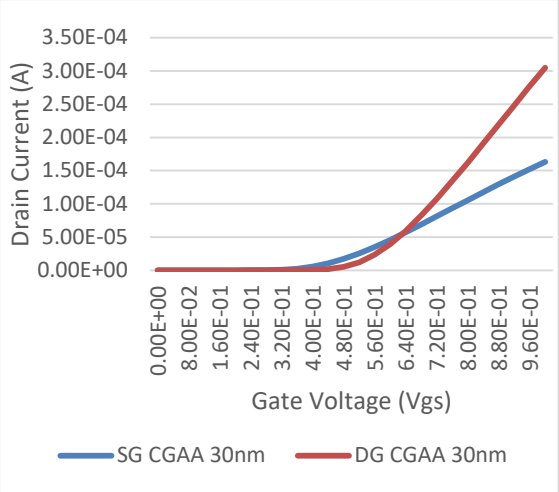

Figure2 : Transfer characteristics of SG CGAA and DG CGAA MOSFET at 30nm channel length

In fig.3. , the transfer characteristics of DMDG CGAA MOSFET is compared with the SG CGAA MOSFET and DG CGAA MOSFET when the gate to source voltage is varied between the 0V to 1V. And drain to source voltage is kept constant V_{DS} = 1V. Drain current is dependent on the metalwork function of the gate electrode. Titanium (Ti) and Aurum (Au) is used as a gate electrode. These two materials are selected for the dual material structure so that the average of the gate electrode can be the same as the single material structure. The higher value of work function (Au = 4.8eV) is situated at the source side and lower value of work-function (Mo = 4.6eV) is situated towards the drain terminal, by using this arrangement of the work function built a step potential channel region [18-19] So the I_D increases in the DMDG CGAA MOSFET than the single material DG CGAA MOSFET and CGAA MOSFET. By using the dual materials in the CGAA MOSFET, also the transport efficiency increases in the DMDG CGAA MOSFET.

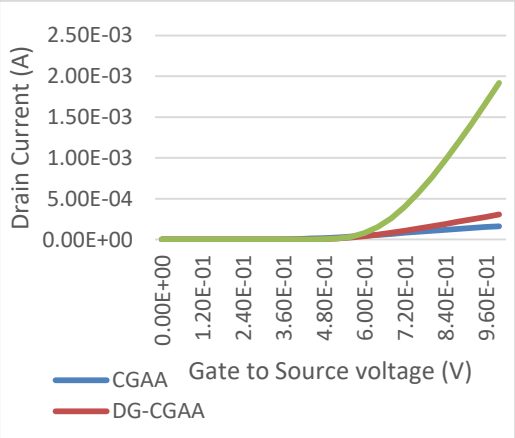

Figure 3: Transfer characteristics of CGAA, DG CGAA MOSFET, and DMDG CGAA MOSFET at 30nm channel length

As shown in Table II, value of the V_{th} is higher for the DMDG CGAA MOSFET than that of the SG CGAA MOSFET and DG CGAA MOSFET. The drain current in the DMDG CGAA MOSFET is also enhanced. As we move for the DMDG CGAA MOSFET from the SG CGAA MOSFET and DG CGAA MOSFET the DIBL also decreases. Thus, by comparing and analyzing the results we can clearly say that DMDG CGAA MOSFET shows better characteristics in all aspects as compared to SG CGAA MOSFET and DG CGAA MOSFET devices.

Table 2: Threshold voltage, drain current, DIBL and transconductance of SG-CGAA MOSFET, DG CGAA MOSFET and DMDG-CGAA MOSFET

MOSFET structure	Vth (V)	Drain current (mA)	DIBL (mV/V)	Trans-conductance (mA/V)
SG-CGAA MOSFET	0.262	0.1628	5.55	0.3
DG-CGAA MOSFET	0.336	0.3052	4.45	0.715
DMDG-CGAA MOSFET	0.363	1.9	3.33	4.90

Fig. 4 shows the transfer characteristics (I_d-V_g) of DMDG-CGAA MOSFET and TMDG-CGAA MOSFET at channel length (L_g = 30 nm). The gate electrode constitutes of three different metals, Aurum (Au) (work- function= 4.8eV), Molybdenum (work- function= 4.6eV) and Titanium (Ti) (work- function= 4.4eV), which have been taken same for TMDG-CGAA MOSFET structures. The above materials have been selected for the triple material structure, this allows us to have the average of the gate electrode to be the same as the single material structure. For dual-material, Molybdenum is discarded from the above three materials. Also, other parameters like oxide thickness (t_{ox}), Silicon thickness (t_{si}), and doping concentrations are taken the same for the comparative study of both the structures. The transfer characteristics are drawn from the constant V_{DS} = 1V and the V_{GS} varies from 0V to 1.0V.

Also, at the gate to source voltage V_{GS} = 1V, the I_D is 1.9 mA and 2.04 mA for DMDG-CGAA MOSFET and TMDG-CGAA MOSFET respectively. The I_D in the TMDG-CGAA MOSFET is greater than DMDG-CGAA MOSFET. In TMDG-CGAA MOSFET, the channel region is wrapped by the triple material gate electrode, allowing the I_D to increase. The introduction of the triple materials enhances the controllability of the gate so that the drain current of the device increases. Because of the surface potential curves and electric field, the threshold voltage is roll-off in the TMDG CGAA structure. But the other SCEs like DIBL is reducing in the TMDG-CGAA MOSFET.

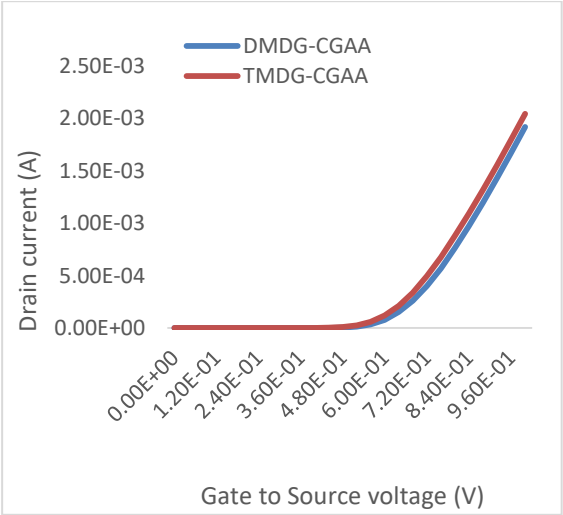

Figure 4: Transfer characteristics of DMDG CGAA MOSFET and TMDG CGAA MOSFET at 30nm channel length

The calculation is done for the various parameters like threshold voltage, DIBL, I_D, and transconductance values. These values are listed in Table III.

Table 3: Threshold Voltage, Drain Current, DIBL, andtransconductance of DMDG CGAA MOSFET and TMDG CGAA MOSFET

MOSFET structure	Vth (V)	Drain current (mA)	DIBL (mV/V)	Trans-conductance (mA/V)
DMDG-CGAA MOSFET (L_G = 30nm)	0.363	1.9	3.33	4.90
TMDG-CGAA MOSFET (L_G = 30nm)	0.346	2.04	1.11	5.82

The design parameters for DMDG CGAA MOSFET and TMDG CGAA MOSFET are taken the same. As the channel, the length is taken 30nm for comparing both the structures, also the other parameters like t_{ox}, $t_{si,}$ etc are the same. From the table, V_{th} is decreased in the TMDG-CGAA MOSFET than the DMDG-CGAA MOSFET. But on current is higher in the TMDG-CGAA MOSFET. The DIBL is also decreased as a move for the TMDG-CGAA MOSFET from the DMDG-CGAA MOSFET. Although the threshold voltage is a little bit lesser in TMDG-CGAA MOSFET the drain current enhances, SCEs (DIBL) reduces and transconductance also improves at the cost of a minor change in threshold voltage. So we can

conclude that the I_D, transconductance is enhanced along with reduced DIBL SCEs by analyzing all the results.

The calculation is done for the various parameters like threshold voltage, DIBL, $I_{D,}$ and transconductance values. These values are listed in Table III. The design parameters for DMDG CGAA MOSFET and TMDG CGAA MOSFET are taken the same. As the channel, the length is taken 30nm for comparing both the structures, also the other parameters like t_{ox}, $t_{si,}$ etc are the same. From the table, V_{th} is decreased in the TMDG-CGAA MOSFET than the DMDG-CGAA MOSFET. But on current is higher in the TMDG-CGAA MOSFET. The DIBL is also decreased as a move for the TMDG-CGAA MOSFET from the DMDG-CGAA MOSFET. Although the threshold voltage is a little bit lesser in TMDG-CGAA MOSFET the drain current enhances, SCEs (DIBL) reduces and transconductance also improves at the cost of a minor change in threshold voltage. So we can conclude that the I_D, transconductance is enhanced along with reduced DIBL SCEs by analyzing all the results.

The threshold voltage (V_{th}) is known as the V_{GS} at which the inversion charge density (Q_{inv}) reaches its threshold value $Q_{th,}$ in gate-all-around devices. We have used Constant Current (CC) method [20] for extracting the threshold value. Where the arbitrary constant current is given by as follows:

$$I_d = \frac{W}{L} \text{x } 10^{-7} \text{ A}$$

Where W and L are the width and length of the channel respectively. Where the formula of effective width is given by:

$$W = 2 \Pi R_{eff}$$

Where the R_{eff} is given as follows

$$R_{eff} = \frac{\int_{R_1}^{R_2} (2\pi r dr) r}{\pi ({R_2}^2 - {R_1}^2)}$$

Here R_1 and R_2 are calculated by the given formulas

$$R_1 = t_c + t_{ox} \text{ and } R_2 = t_c + t_{ox} + t_{si}$$

Where the t_c is core diameter, t_{ox} and t_{si} are thicknesses of the oxide and silicon respectively. By using the constant current method (CC method), the value of the threshold voltage can be taken out. By using this method the V_{th} can be measured corresponding to a constant current, on this constant current the value if V_{GS} is known as the threshold voltage (V_{th}) [21].

DIBL is known as the V_{th} variation at V_{DS}= 0.1v and V_{DS}= 1.0 to the V_{DS} variation V_{DS}= 1v and V_{DS}= 0.1v.

$$DIBL = \frac{\Delta V_{th}}{\Delta V_{DS}} = \frac{(V_{th})_{V_{ds}=0.1v} - (V_{th})_{V_{ds}=1v}}{(V_{ds} = 1v) - (V_{ds} = 0.1v)}$$

The unit of the DIBL is mV/V.

Transconductance is determined by the ratio change in I_D to the change in V_{GS}. $g_m$is the symbol and the unit is mA/V for the transconductance. In short higher transconductance gives higher amplifications. Transconductance can be calculated by the transfer characteristic of the device. The formula used for the transconductance is given as follows:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{(I_D)_{V_{gs}=1v} - (I_D)_{V_{gs}=0.8v}}{(V_{gs} = 1v) - (V_{ds} = 0.8v)}$$

The I_{on} current is the drain current which is obtained while the transistor is working in its on the state. And I_{off} current is obtained when the transistor is working in the off state. An ideal situation for an ideal switch, the on-current is limited by the external circuit and the off current is ideally zero. But practically the off current is not zero but it has to be minimized for the better switching characteristics. In the planar MOSFET at 30nm channel I_{off} enhances, so for reducing the off current in the MOSFET in the nanometer region also, we have designed the CGAA MOSFET. In the SG-CGAA MOSFET, the off current is decreasing then the planar MOSFET at 30nm channel length. At 30nm in the planar MOSFET I_{off} is 5e-4 A which was too close to its current. So the device fails to maintain the I_{on}/I_{off} ratio range. And in the SG-CGAA MOSFET, the off current is 6.79e-12 A, which is very low than the planar MOSFET. The off current is minimized in the CGAA structure. In the DG-CGAA MOSFET, the channel is controlled by two gates (inner and outer) so the gate controllability and I_{on} enhances and I_{off} current reduces. In the CGAA and DG-CGAA MOSFET the off current minimizes but the on current was also low but in the triple material drain current also improves. In triple material, the off current is obtained 7.73e-13 A, which is the lowest among these structures and also the drain current is improved by the influence of the three materials.

The on-current is maximum in the TMDG-CGAA MOSFET and the off current is lowest in the TMDG-CGAA MOSFET. So, according to fig5, we can say that by the introduction of the material engineering in the gate engineering the I_{on}/I_{off} ratio improves. Because in the TMDG-CGAA MOSFET the gate controllability is increased than the CGAA MOSFET and DG-CGAA MOSFET. And the I_D is dependent on the work function. By the work-function arrangement in the triple material creates a step potential in the channel region. Multiple materials so used instead of single material in the gate electrode, allows the transport efficiency to increase in the channel region. So, the I_{on}/I_{off} ratio improves in the TMDG-CGAA MOSFET.

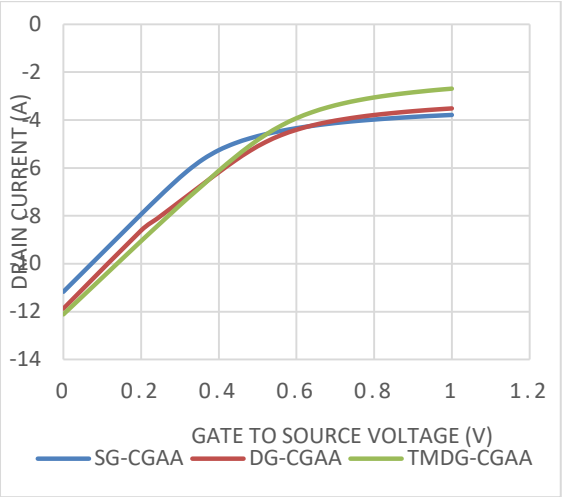

Figure 5 : Drain current (in Log scale) to V_{GS}, at $V_{DS,}$ = 1.0V of SG-CGAA MOSFET, DG-CGAA MOSFET and TMDG-CGAA MOSFET at 30nm channel length

Table 4: I_{on}/I_{off} ratio values of SG-CGAA MOSFET, DG CGAA MOSFET, and TMDG CGAA MOSFET

MOSFET structure	I_{on}/I_{off} ratio
SG CGAA MOSFET	2.40×10^{7}
DG-CGAA MOSFET	2.27×10^{8}
TMDG-CGAA MOSFET	0.3×10^{10}

8. CONCLUSION

In the proposed design MOSFET, DIBL is reduced to 1.11mV/V at channel length 30nm. The ratio of I_{on}/I_{off} is also improved in the proposed design. Whereas in the planar MOSFET the off current also increases, due to the SCEs was arisen, and also the planar MOSFET was not able to sustain the acceptable range of the I_{on}/I_{off} ratio for the same channel length at 30nm. Transconductance is also improved in this structure. So we can conclude that by using the double gate cylindrical structure and materials the SCEs are reduced effectively in proposed TMDG-CGAA MOSFET.

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