Simulation and Boolean Expression Verification of Ultrahigh Speed Optical Logic Gates using SOA-MZI Structure

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Abstract:Optical networks are the key elements in demanding all-optical logic devices. This paper gives the detailed description of AND, OR, NOT & NAND gates designs simulations based on nonlinear element Semiconductor Optical Amplifier Mach Zehnder Interferometer structure. The FWM, XGM, XPM nonlinearity forms are used to achieve the ultra-highspeed (40Gbps) and Boolean expression of logic gates. Refractive index of SOA changes, due to the nonlinear character of the semiconductor optical amplifier which produces a high gain for ultra-high speed (40Gbps) of all logic gates. These proposed logic gates operate at 10Gbs (input data rate). The entire work is performed on the Opti system software for component analysis and Boolean expression testing. Realization of Boolean expression with high Q factor and ultrahigh speed operation and reconfiguration of logic gates is performed here.

Keywords:Semiconductor Optical Amplifier-Mach Zehnder Interferometer (SOA-MZI), Cross Phase Modulation (XPM), Cross Gain Modulation (XGM).

1. INTRODUCTION

The SOA is a nonlinear amplifier and this nonlinear character is used for simulation of different optical logic gates. Logic gates are used for multiplexing (add and drop), signal processing, address recognition and packet synchronization [1]. SOA makes a high-level change in the refractive index and gives output gain with ultrahigh speed (40Gbps). SOA is an optoelectronic device that amplifies light signals. Due to this property of SOA, this can be used in various applications of logic gates to achieve high output saturation power, high output gain, low polarization dependence, and minimal facet refractivity. The best feature of this device is signal regeneration. The Mach Zehnder Interferometer (MZI) is mostly used in the implementation of all high-speed logic gates [2]. The XOR, NOR and AND gates operated up to10Gbps with the help of nonlinear optical amplifier with MZI structure. To simulate the digital operations, many structures of optical logic gates are used like the ultrafast non-linear properties of detuning optical band pass filter and SOA.

Nonlinearities of Logic Gates Based on SOA

SOA is essentially nonlinear. Nonlinearities given by SOA may be used to implement all kinds of optical logic gates.

Nonlinearity has three major types: -

1.1 XGM (Cross Gain Modulation): In XGM all input signals are affected homogeneously due to variations in the density of carriers in the optical amplifiers. If the input power is increased, the carrier density in SOA gets depleted which reduces amplification gain [2]. The dynamic process is in the order of picoseconds (very fast) that is responsible for changes in semiconductor optical amplifier Density. This change can be used bit by bit gain fluctuation of the input signal power [3].

1.2 XPM (Cross Phase Modulation): In XPM all active region refractive index is not constant in the semiconductor optical amplifier, but it depends on the carrier density and the material gain. The preceding condition indicates that the gain and phase of the optical wave which propagates in the optical amplifier is coupled by gain saturation. By MZI configuration, phase modulation changes in intensity modulation.

1.3 FWM (Four Wave Mixing): Four wave mixing is the third-order nonlinear process. When two or more wavelengths combine, then it can produce one or more wavelengths. The nonlinearities properties XPM and XGM of SOA are used in the design of logic gates.

2. METHODOLOGY

The methodology proposed in the paper is based upon cross gain modulation. This is shown in Fig.1. The figure shows the wavelength conversion semiconductor optical amplifier which includes pump source, CW probe, SOA, Gaussian filter, and modulated probe for output. SOA is a nonlinear element that exhibits strong changes in the refractive index and gives high gain.



Figure 2: Wavelength conversion in SOA

In cross gain modulation, there are two input signals, one is a probe light, and another is a pump light. Probe light is weak and pump light is strong which has a less harmonic signal modulation, modulates at ω (angular frequency), both are given at the same time [4]. Pump modulation on the probe is enforced to the amplifier using XGM. Due to this, amplifier acts as a wavelength converter means a signal having one wavelength is fed to another signal having other wavelengths [4]. These technologies are used in the simulation of logic gates.

3. RESULTS AND DISCUSSION

Parameters used in the simulation of logic gates are - SOA pump signal power, SOA probe signal power, wavelength for pump signal, wavelength of the probe beam, length of SOA, width of SOA, injection current of SOA, optical confinement factor. These parameters are used in Opti system software in designing of logic gate which are selected from base paper [5]. The parameters used for the simulation of different logic gates proposed in this paper are mentioned in Table I.

| Table 1: Designing parameters of SOA for simulation of logic | |
|--|--|
|--|--|

| Domomotors | Value For | Value For | Value For |
|-------------------------------|--------------|-------------|-----------|
| r ai aineter s | AND GATE | NOT GATE | OR GATE |
| SOA pump signal power | 0.5mw | 0.3 mw | 0.5mw |
| SOA probe signal power | 0.25mw | 0.25 mw | 0.25mw |
| Wavelength for pump signal | 1545nm | 1550nm | 1550nm |
| Wavelength for the probe beam | 1548nm | 1540nm | 1545nm |
| SOA length | 0.0005 | 0.0005 | 0.0005 |
| Width of SOA | 3e-006 | 3e-006 | 3e-006 |
| Injection current of SOA | 0.35A | 0.35A | 0.35A |
| SOA optical confinement | 0.4 | 0.5 | 0.5 |

3.1 Implementation of AND Gate :

factor

If both input AN_1 and AN_2 are one then output is one (if $AN_1 = 1$ or $AN_2=1$), otherwise, we get output logic zero in all conditions (if $AN_1=0$ or $AN_2=1$ and $AN_1=1$ or $AN_2=0$ and $AN_1=0$ or $AN_2=0$). The Gaussian filter frequency is set at 1550 nm for simulation of AND gate. The Boolean verification of this gate is given in Table II. The theoretical result has been shown through Boolean table and practical result have been shown through graphs and they both are



matching. The layout used for gate simulation is shown in Figure 2.

Figure 2: AND Gate Layout





Figure 5: OUTCOME (0101)

3.2 Implementation of OR Gate :

If both input OR_1 and OR_2 are zero then output is zero (if $OR_1=0$ or $OR_2=0$), otherwise, we get output logic one in all conditions (if $OR_1=0$ or $OR_2=1$ and $OR_1=1$ or $OR_2=0$ AND $OR_1=1$ or $OR_2=1$). The Gaussian filter frequency is set at 1550nm for simulation of the OR gate. The Boolean verification of this gate is given in Table III. The theoretical result has been shown through Boolean table and practical result has been shown through graphs and they both are matching. The layout used for gate simulation is shown in Figure 6.



Figure 6: OR GATE layout





| Table3:.Boolean verification | | | | |
|------------------------------|-----------------|---------|--|--|
| OR ₁ | OR ₂ | OUTCOME | | |
| $OR_1 low (0)$ | $OR_2 low(0)$ | 0 | | |
| $OR_1 low (0)$ | OR_2 high (1) | 1 | | |
| $OR_1high(1)$ | $OR_2 low (0)$ | 1 | | |
| $OR_1high(1)$ | $OR_2high(1)$ | 1 | | |

3.3 Implementation of NOT gate:

In this output always invert of the input signal that is if the input signal is zero then output is 1 and input is 1 then output is zero. The gaussian filter frequency is set 1550 nm for simulation of NOT gate.



Figure 8 NOT gate layout



| INPUT NR ₁ | OUTCOME |
|-----------------------|---------|
| 1 | 0 |
| 0 | 1 |

3.4 Implementation of NAND gate

It gives output logic high (1) when any input logic is low (0) and gives output logic low (0) when both inputs are the same high (1). The Boolean verification of this gate is given in Table V. The layout used for gate simulation is shown in Fig.



Figure 11NAND gate layout

4. CONCLUSION

For an ease of solution availability for logic gates designs, SOA-MZI structure is used. The principle of operation, multiple simulation steps, inputs, and

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outputs are described systematically in the proposed paper. In this paper, the results of inputs and output simulation are compared with theoretical inputs and output results, it has been analyzed that all are matching exactly. The major application of these gates is in optical networking. The gain of this proposed system is at 10 Gbps (input data rate) and provides a high gain with ultrahigh speed (40Gbps).In this work; Realization of Boolean expression with high Q factor and ultrahigh speed operation and reconfiguration of logic gates is done. The theoretical results have been shown through Boolean table and practical results have been shown through graphs and they both are matching.





Table 5. Boolean verification

| NA ₁ | NA ₂ | OUTCOME |
|--------------------------|-----------------|---------|
| $NA_1 low(0)$ | $NA_2low(0)$ | 1 |
| $NA_1 low(0)$ | $NA_{2}low(0)$ | 1 |
| NA ₁ high (1) | NA_2 high (1) | 1 |
| NA ₁ high (1) | NA_2 high (1) | 0 |

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