Effect of SiO_2 Thickness Variation on Threshold Voltage and Trans-Conductance of TFT

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***Abstract*- In this study bottom-gate oxide IGZO thin film transistors have been simulated and the SiO_2 dielectric material thickness variation had been investigated. The IGZO bottom gate TFT was simulated using Silvaco TCAD software. The electrical parameters threshold voltage and Trans conductance was observed with an active layer thickness 30nm, channel length is 5 μm and the variation of thickness of $SiO_2$from 40nm to 140nm.Threshold voltage and transconductance decreased with the increase of the SiO_2 thickness.**

Keywords: Threshold voltage, Transconductance, Channel length

1. INTRODUCTION

Oxide-based thin film transistors have been investigated for a number of applications, including switching components in flat panel display backplanes, gas sensor applications, and UV detecting devices. Thin film transistors are made by depositing a thin layer containing a dielectric material on a variety of substrates, such as plastic, fibre, paper, and silicon [1-3], and then removing it. The contact between the semiconductor layer and the source, drain, and gate is established by the source, drain, and gate. The four types of device architectures are bottom gate top contact, bottom gate bottom contact, top gate top contact, and top gate bottom contact. Bottom gate top contact is the most common device structure. The bottom gate top contact design is the most successful of the four designs studied for small molecules-based transistors. [4]. An oxide-TFT exhibits good homogeneity and mobility in the centre of the spectrum between a-Si and LTPS. Oxide-TFT offers greater film uniformity and lower processing temperatures than traditional TFT, making it suitable for large-area applications with low production costs and large-sized LCD panels [5-10].

TFTs based on indium gallium zinc oxides enhanced the TFT's electrical performance. Transparent thin-film transistors using indium–gallium–zinc oxide (IGZO) active channel layers have gained popularity in recent years because to their low threshold voltage, high transconductance, and greater Ion/Ioff current ratio. Because of their optimum threshold voltage and high transconductance, these transistors offer excellent switching properties. The choice of gate dielectric materials that fit the thin layer of semiconductor materials is an analytic problem for improving the electrical properties of TFTs [12-13]. In this paper, we investigated TFT using 2-D device simulation and reported the effect of dielectric SiO2 thickness on electrical parameters threshold voltage and transconductance of IGZO based TFT.

2. DEVICE STRUCTURE AND SIMULATION METHOD

Fig. 1 depicts an enlarged simplified two-dimensional cross-section of the staggered bottom-gate a-IGZO TFT device structure that was utilised in this research. It is possible to simulate the functioning of the a-IGZO TFT by utilising a Silvaco Atlas simulator on a two-dimensional grid, which is made up of a number of finite element grid points, which are referred to as nodes.

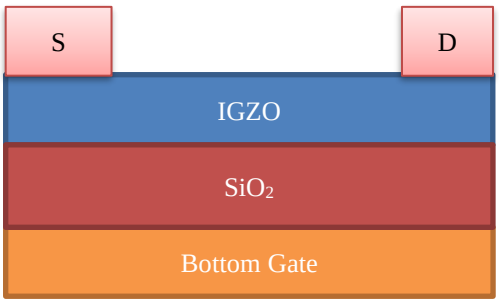

Fig. 1 Structure of bottom gate IGZO TFT devices

Atlas simulates the movement of carriers through the structure by solving a set of differential equations (Poisson's and continuity equations) on this grid [13]. The connection between the charge held inside the crystal and the electric field generated as a consequence of this surplus charge, as well as the resultant electric potential, is described by Poisson's equation.

Carrier density varies with time due to the difference between the incoming and outgoing carrier fluxes, as well as generation and recombination. This shift in carrier density is explained by the continuity equation. The continuity equations for free electrons and holes in steady state, obtained by ignoring the generation rate, are provided by- and-

$$\frac{1}{q} div \overrightarrow{J_n} - R_n = 0$$

$$-\frac{1}{q} div \overrightarrow{J_p} - R_p = 0$$

Where, the electron and hole current densities are denoted by the symbols Jn and Jp, respectively.
The electron and hole recombination rates are represented by the letters Rn and Rp, respectively. Let n and p denote the low field electron and hole mobility, respectively, and EFn and EFp denote the electron and hole quasi-Fermi levels, respectively.
The current densities in the drift-diffusion model are given by the equation [1]:

$$J_n = -q\mu_n n \nabla E_{Fn}$$

$$J_p = -q\mu_p p \nabla E_{Fp}$$

3. EFFECT OF SiO_2 THICKNESS VARIATION

Threshold voltage of the thin film transistor decrease with increasing channel thickness [2].The effect of SiO2 thickness on the electrical properties of proposed device was observed for constant channel length L=5 and 30nm thickness of IGZO semiconductor materials and drain voltage is Vd=2V. The thickness of SiO2 is varied from 40nm to 140nm and observed the effect on threshold voltage and trans-conductance. The simulation was started with the channel length of 5 micrometer.

Table 1: Variation of SiO2 thickness and observed threshold voltage, trans-conductance and on/off current

S. No.	SiO_2 Thickness (nm)	Threshold Voltage (V)	Trans-conductance (μs)
1	40	0.77	111.31
2	50	0.76	89.08
3	60	0.74	74.14
4	70	0.72	63.49
5	80	0.69	55.47
6	90	0.67	49.23
7	100	0.64	44.24
8	110	0.61	40.17
9	120	0.58	36.78
10	130	0.56	33.91
11	140	0.54	31.46

The trans-conductance is a transfer coefficients relating output current to input voltage. In the TFT the input voltage is gate to source voltage V_{GS} and output current is drain current I_D. This is a used to determine the gain of transistors.

$$g_m = \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}=constant} = \frac{\varepsilon_0 \varepsilon_r}{T_{ox}} \mu_n \frac{W}{L}(V_{GS} - V_T)$$

If the thickness of the dielectric layer (T_{ox}) increases, then the transconductance (g_m)decrease [16].
We observed the variation in transconductance with respect to SiO2 thickness. Analyzed simulation result, as the value of trans-conductance of the present sample is initially 111.31 μS at 40nm SiO2 thickness. After the value of transconductance decreased with increase in the SiO2thickness and reached minimum of 31.46 μS at 140 nm. The variation of trans-conductance with respect to SiO2 thickness is shown in Fig 2.

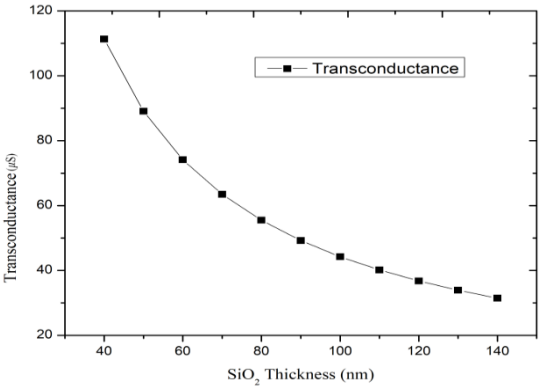

Fig. 2 Trans-conductancevs SiO_2 Thickness

The threshold voltage (VT) of the devices is defined as the lowest gate voltage needed to produce a significant buildup of charge. When the line is extended to zero drain current, it is possible to find the intercept with VGS, which is the value of the threshold voltage.
When scaling reaches the nanometer regime, the threshold voltage decreases as the oxide thickness is increased. A precise simulation requires the incorporation of two ideas. The first point to make is that the channel depletion area contains hundreds of impurity atoms. Intrinsic dopant oscillations are responsible for the threshold voltage's considerable dispersion. Second, quantum confinement inside the channel has a substantial effect on the threshold voltage [17].
Fig 3 shows the variation in Threshold voltage with respect to SiO2 thickness. The value of threshold voltage is 0.77 V at 40 nm SiO2 thickness and it decreased with the increase of SiO2 thickness.

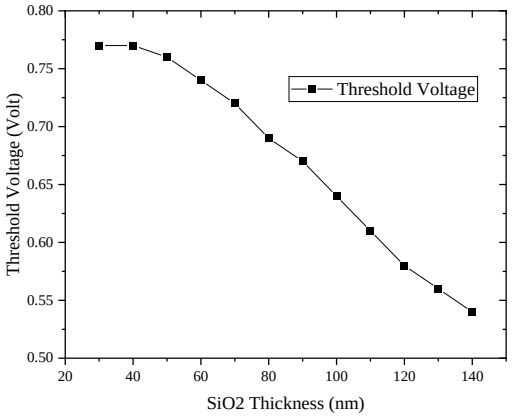

Fig. 3 Threshold voltage vs SiO_2 Thickness

As stated in the Enhancement mode behavior of the n channel bottom gate TFT in Fig 4, the transfer

characteristics of TFT in between ID and VGS are shown in the Fig 4. The transfer properties are investigated for a variety of drain to source voltage combinations. When the voltage between the drain and the source rises, the drain current increased.

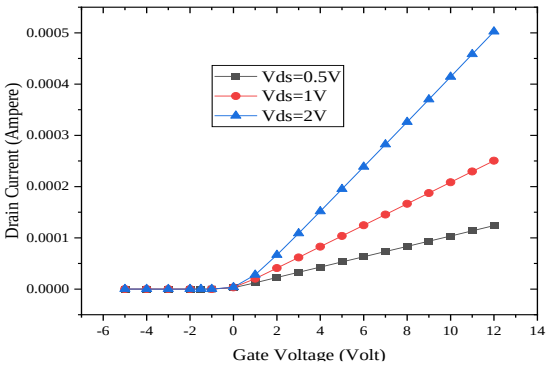

Fig. 4 Transfer characteristics of TFT: Drain current vs Gate voltage

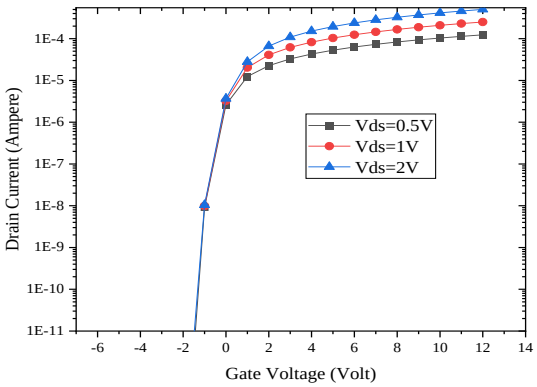

Fig. 5 Transfer characteristics of TFT: Drain current in log scale vs Gate voltage

4. CONCLUSION

An IGZO TFT was simulated using Silvaco TCAD tool. We simulated the relationship between the threshold voltage and transconductance with the thickness of Dielectric SiO2.

The active layer thickness was taken 30 nanometre and SiO2 was taken as a low K dielectric material .The thickness of SiO2 was varied from 40nanometre to 140 nanometre and threshold voltage and trans-conductance were observed.

The present study examined the trans-conductance of TFTs and concluded that the trans-conductance dropped as the SiO2 thickness increased. The threshold voltage decreases as the SiO2 thickness increases. We observed the IDS-VGS transfer characteristics of TFT and examined the drain current, increase with increase the Drain to source voltage VDS.

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