Effect of Scaling on Device Characteristics of Triple Material Double Gate (TMDG) Strained Channel NMOS

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Abstract: **In this paper effect of scaling on a TMDG strained channel Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is analyzed. To observe the scaling effects we have designed MOSFETs with varying channel lengths i.e. in the ratio of 2:3:4. In our previous paper we have designed a Triple Material Double Gate (TMDG) strained channel MOSFET to improve performance of nano scaled transistors. Here, we have analyzed the effect of reduction in channel length of the TMDG strained channel MOSFET. For this we have designed MOSFETs of 60nm, 45nm and 30nm channel lengths, and electrical characteristics like threshold voltage and trans-conductance (g_m) are also calculated for these transistors. Short channel effect parameter DIBL is calculated for the MOSFETs using Constant Current (CC) method, which shows increased SCEs in smaller channel length transistors. Comparative analysis of surface potential profiles of these transistors shows reduced threshold voltage (V_{th}) in scaled MOSFETs.**

Keywords: TMDG MOSET, Strained-Si Channel, Drain Induced Barrier Lowering (DIBL), Short Channel Effects (SCEs), Surface Potential Profile, trans-conductance (g_m).

1. INTRODUCTION

As we know for designing of high packing density chips in MOS VLSI technology, sizes of transistors should be as small as possible. Reduction of sizes or dimensions is commonly referred as scaling of transistors. Extent of scaling of MOSFETs strongly depends on the fabrication technology or on the minimum feature size of that technology node. Electrical characteristics of devices changes with the reduced dimensions. For example: nano-scaled MOSFETs or short channel MOSFETs show strong deviation in device characteristics from that of long channel MOSFETs. So modifications in MOS device structure and conventionally used materials are required to reduce variations in characteristics of short channel MOSFETs [1-5]. In order to reduce these short channel effects, a Triple Material Double Gate (TMDG) strained channel MOSFET with 30nm channel length was introduced in our previous paper. In this paper, Effects of scaling on this MOSFET are explained in detail. TMDG structure of the MOSFET shows reduced DIBL performance due to three different work-function materials in both gate electrodes and strained silicon channel shows improved trans-conductance performance. As we know, Reduction in the dimensions of a MOSFET takes place together with corresponding increase of doping densities. Increased doping densities degrade surface mobility of MOSFET due to scattering of charge carriers. Strained-Si devices show better immunity against mobility degradation, because Silicon thin film grown over a relaxed $Si_{1-x}Ge_x$ substrate experiences biaxial tension or strain due to lattice mismatch. Due to strain, the electron affinity of silicon increases and the band-gap decreases, as a consequence effective mass of carriers in Si also decreases, which leads to increased mobility in silicon [6-10].

1.1 Scaling of MOS Transistors

Scaling of MOS transistors is a systematic reduction in all three dimensions of the device, as allowed by the available technology. Overall function density of the chip increases due to scaling because reduction in the total silicon area occupied by a single transistor reduces. For scaling of MOSFET, all horizontal and vertical dimensions of the large size transistor are divided by constant scaling factor ($S > 1$) [1]. According to Moore's law, new generation manufacturing technology replaces the previous one in about every two years. It is also observed that and the downscaling factor S of the minimum feature size from one generation to the next is about 1.2 to 1.5. Scaling of all dimensions by a factor of $S > 1$, reduces the area of the transistor by a factor of S^2.To better understand

the effect of scaling on the current-voltage characteristics of the MOSFET two different scaling strategies are as follows:

1.1.1 Full Scaling or Constant Field Scaling

In this scaling strategy all physical dimensions are reduced by the scaling factor in such a way that internal electric field remains constant. For this all the potentials in the MOS circuits are also reduced by the same scaling. As we know dissipated power of transistor is given by the multiplication of drain current and voltage. Both drain current and voltage are reduced by a factor S, so dissipated power reduces by a factor of S^2. Significant reduction in the dissipated power is an attractive feature of full scaling.

1.1.2 Constant Voltage Scaling

As in full scaling, voltage is scaled down by the scaling factor but Scaling of applied voltages is not practically possible in many cases because additional peripheral circuitry may be required for certain voltage scaling. Also reduction in voltage levels increases the delay of circuit. So Constant Voltage scaling strategy is preferred over full scaling strategy. In this strategy physical dimensions are scaled down by a factor S with the constant voltages and doping densities of the channel and source/drain regions are increased by the factor of S to preserve charge-field relations. As In this paper, Effect of the variation in channel length of MOSFET is observed so all other parameters are kept unchanged [2].

1.2 Short Channel Effects in MOS Devices

A MOSFET device is considered to be short when the channel length is of the same order of magnitude as the depletion-layer widths (x_{dD},x_{dS}) of the source and drain junction. As the channel length L is reduced to increase both the operation speed and the number of components per chip, the so-called short-channel effects arise. As device geometries of MOS transistor are continuous reducing in nano-meter regime, Electrical properties show strong deviance from long channel MOSFET performance [11-14]. These deviances occurring due to decrease in channel length are known as SCEs (Short channel Effects). Short Channel Effects results in significant changes from ideal characteristic of conventional transistors like drain source series resistance, channel length modulation, carrier velocity saturation, Hot Carrier Effects (HCEs), drain induced barrier lowering (DIBL), and punch through [3].

2. DEVICE STRUCTURE

Triple Material Double Gate (TMDG) strained Si (s-Si) channel n-MOSFET structures of 30 nm, 45 nm and 60 nm channel lengths are shown in fig.1, fig.2 and fig. 3 respectively, which are designed using ATLAS tool. Both gate electrodes of all the MOS structure have three materials namely $\mathbf{Au(\varphi_{m1} = 4.8eV), Mo(\varphi_{m2} = 4.6eV)}$ and $\mathbf{Ti(\varphi_{m3} = 4.4eV)}$ deposited over equal lengths. Channel region of the devices is lightly P-doped strained silicon with acceptor concentration (N_A) = 1×10^{16} cm^{-3}.

Source and Drain regions are highly doped with donor concentration (N_D) = 1×10^{20} cm^{-3}. As the effect of channel length is to be observed in TMDG strained channel MOSFET, so all other parameters are kept unchanged. Design parameters of these transistors are as shown in table 1.

All three materials in gate electrodes are deposited over equal lengths i.e. in 30nm channel length NMOS aurum, molybdenum and titanium are deposited each for10nm, In 45nm each is deposited over 15nm and in 60nm channel length NMOS these are deposited for 20nm length.

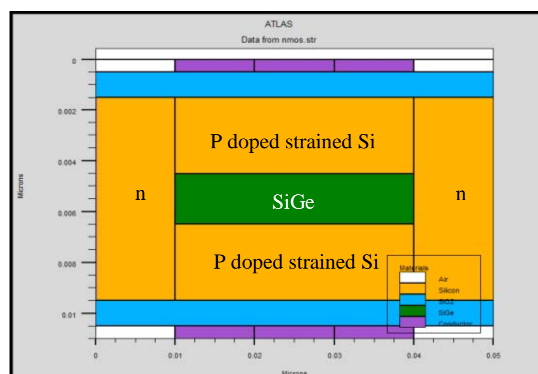

Figure 1: TMDG strained Si (s-Si) channel n-MOSFET of 30nm channel length

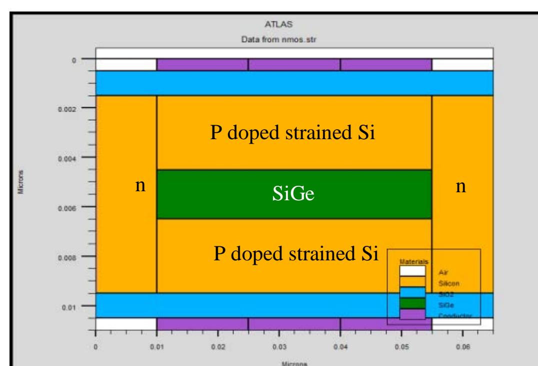

Figure 2: TMDG strained Si (s-Si) channel n-MOSFET of 45nm channel length

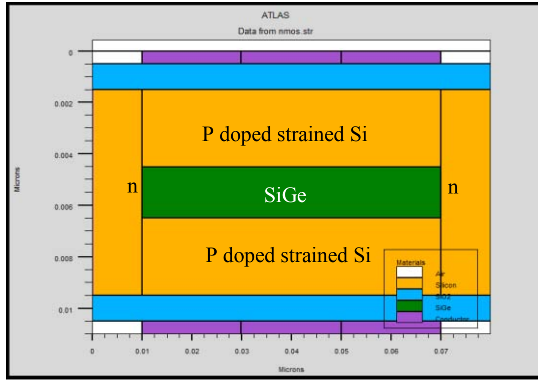

Figure 3: TMDG strained Si (s-Si) channel n-MOSFET of 60nm channel length

Table 1: Typical Design Parameter Values

Parameters	Values
Upper and Lower Gage oxides (t_{ox})	2 nm
Channel Doping Concentration (N_A)	1×10^{16} cm^{-3}
Source and Drain Doping Concentration (N_D)	1×10^{20} cm^{-3}
Work-function of Metal1 Au ($\boldsymbol{\varphi_{m1}}$)	4.8 eV
Work-function of Metal2 Mo ($\boldsymbol{\varphi_{m2}}$)	4.6 eV
Work-function of Metal3 Ti ($\boldsymbol{\varphi_{m3}}$)	4.4 eV
Channel Lengths of transistors (L_g)	30 nm, 45 nm and 60 nm

3. RESULTS

Fig. 4 shows the drain current (I_d) as a function of gate to source voltage (V_{gs}) i.e. transfer characteristics for TMDG n-MOSFET with strained Si (s-Si) channel of 30nm, 45nm and 60nm with constant drain voltage (V_{ds}= 1volt) and gate voltage varying from 0 volt to 1.5 volt.

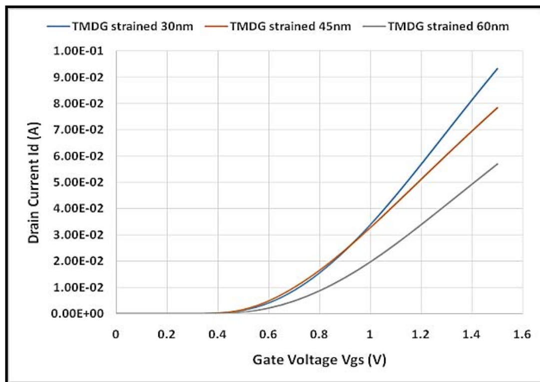

Figure 4: Transfer characteristics of MOSFETs

From transfer characteristics of MOSFETs (Fig. 4), we can observe that, at gate to source voltage 1.5 V drain current 57.08 mA, 78.51 mA and 93.37 mA is obtained for 60nm NMOS, 45nm NMOS and 30nm NMOS respectively, which shows that drain current increases when we scale down channel length of MOSFET.

The threshold voltage (V_T) is a fundamental parameter which shows the gate voltage value at which onset of significant drain current flow takes place in the MOSFET channel. For evaluation of threshold voltage (V_{th}) we have used constant current (CC) method. This method evaluates the threshold voltage as the value of the gate voltage (V_g), corresponding to a given arbitrary constant drain current, I_D and V_d < 100mV. A typical value for this arbitrary constant drain current is chosen as $\frac{W}{L} \times 10^{-7}\, A$, where W and L are the channel width and length, respectively [15-18].

For an MOSFET, Trans-conductance is defined as the ratio of the change in gate voltage to the change in gate voltage. In general, larger the trans-conductance shows greater the gain or amplification capabilities. Trans-conductance of the MOSFETs is calculated using drain current at two different gate to source voltages.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{(I_D)_{V_{gs}=1v} - (I_D)_{V_{gs}=0.8v}}{(V_{gs} = 1v) - (V_{ds} = 0.8v)}$$

Table 2: $\mathbf{V_{th}}$, $\mathbf{g_m}$ and DIBL Values of TMDG Strained MOS at 30 nm, 45nm and 60 nm Channel Length

MOSFET Structure	DIBL (mV /V)	g_m (mA /V)	$V_{th}(V)$
TMDG strained channel MOSFET (L_g=60nm)	1.11	55.10	0.209
TMDG strained channel MOSFET (L_g=45nm)	2.00	81.25	0.162
TMDG strained channel MOSFET (L_g=30nm)	4.45	91.50	0.128

Table 2 shows the calculated values of threshold voltage ($\mathbf{V_{th}}$), trans-conductance ($\mathbf{g_m}$) and Drain Induced Barrier Lowering (DIBL) for 60 nm, 45 nm and 30 nm channel length TMDG strained channel MOSFETs.

From table 2, we can conclude that when we scale down MOS transistors to next technology node, trans-conductance increases with the reduction in channel length. Particularly from table, we can see that when channel length is reduced from 60nm to 45nm, trans-conductance increases from 55.10 mA/V to 81.25 mA/V and at 30 nm channel length it has been reached to 91.50 mA/V, which is a high value and show higher gain or amplification capability of transistor.

In order to see the adverse effects of the scaling in nano-meter regime, DIBL is calculated for the MOSFETs. Drain induced barrier lowering (DIBL) is one of the undesirable effects, which occur in short channel MOSFETs [19-20]. The change in the threshold voltage due to the variance of drain voltage ($\Delta \mathbf{V_{th}}$), is calculated as Drain induced barrier lowering (DIBL). DIBL of the MOSFETs is calculated using threshold voltage at two different drains to source voltage. Threshold voltage for different $\mathbf{V_{DS}}$ are calculated by constant current method [21].

$$DIBL = \frac{\Delta V_{th}}{\Delta V_{DS}} = \frac{(V_{th})_{V_{ds}=0.1v} - (V_{th})_{V_{ds}=1v}}{(V_{ds}=1v) - (V_{ds}=0.1v)}$$

From the DIBL values of the MOSFETs, it is concluded that for long channel MOSFETs short channel effects are almost negligible, and when we move from 45 nm channel length to 30 nm channel length DIBL almost has been doubled.

Fig. 5 shows surface potential profile of the MOSFETs. From surface potential profile we can conclude that at 30 nm channel length MOSFET, potential barrier from source to drain has been reduced from that of 60 nm channel length MOSFET. Also surface potential of all three MOSFETs show steps at the interface of two materials, two steps are observed in the profile due to three materials in gate electrodes of the transistors. Reduced potential barrier in 30 nm channel length NMOS, shows reduced threshold voltage of the transistor, which can also be observed from table 2.

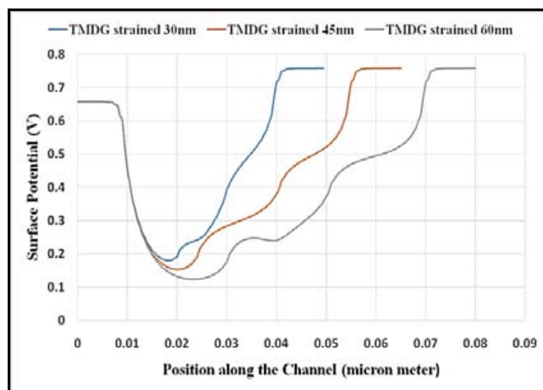

Figure 5: Surface Potential Profile of MOSFETs

4. CONCLUSION

From the results obtained we can conclude that scaling of the MOSFETs leads to increased Short Channel Effects (SCEs) so as increased DIBL. Also threshold voltage roll off is seen in scaled transistors. Drain current of the MOSFET in scaled device also increases drastically, As a result trans-conductance of MOSFETs increases. Overall, Scaled devices in high density chips show better performance as compare to their long channel counterparts, except increased Short Channel Effects. These SCEs are also compensated with modified structure and materials.

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