

Designing High Speed 64 bit Multiplier using Vedic Sutra

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Abstract: Vedic multiplier is a unique and prompt multiplier dependent on Vedic mathematics. The main component used in this procedure is adder. Vedic multiplier's performance can be enhanced by using fast adder. Hence in this paper we are using 64*64 bit multiplier using 32-bit Vedic multiplier and getting path delay lowest. For finding value of 64-bit multiplier, we need 32-bit multiplier for multiplication. Here we are applying Vedic Mathematics Sutra called "URDHVA TIRYAKABHYAM" for proposed 64*64 bit multiplier in Xilinx ISE 14.7. This design does not take more time for execution of the operation than comparison with available multiplier. This Vedic method is effective to improve the speed of image processing and digital signal processing. It works on high speed with great performance. This technique includes different types of wide area of image and digital signal processing. At the end, the result of proffered multiplier is compared with 64-bit multiplier using different adders.

Keywords: Ancient Vedic mathematics, Urdhva-Tiryakbhyam Sutra, Vedic real multiplier, Kogge- Stone Adder (KSA), Xilinx ISE 14.7, VHDL.

1. INTRODUCTION

Word "Vedic" is taken from "Veda" which is shown as one of most prepared method of acquiring knowledge. Vedic Mathematic is fit to solve any mathematical issue at a very high speed with few steps. The concept of Vedic mathematics is originated from "Atharva Vedas". In applied sciences, Vedic mathematics is mostly use.

Vedic Mathematic has sutras and sub sutras. These sutras present undercover reinforcement strategy systems to all essential intelligent errands. The strong application of Vedic science is in 'sequence of numbers'. It fuses for all intents and purposes all pieces of science.

The convincing employments of Vedic Science have shown in an area's upgraded speed similarly as Less Power figuring related with VLSI Math undertakings, Computerized Signal Preparing, Discrete Fourier Change techniques, Chip Structuring strategies, and encoding of main

structure. Digital Signal Processing (DSP) technique are immense part in building discipline. DSP errands can be realized in number of ways and methodology. Association and Complications are some main tasks in DSP where capable duplication is required.

Configuration of Vedic multiplier has given this straight imposition to assemble increment quickly when diverged from customary techniques. This paper depicts chart and attainment of snappy propagator. Vedic science-based parts with different utilitarian squares can sort out in an ALU to perform snappy duplication. Such number shuffling basis unit will be on a very basic level suitable when diverged from the standard ALU.

2. USABILITY

A multiplier is a foundational auxiliary module in Digital signal processing (DSP) and Arithmetic logic units (ALU). Present day age processors capacities at quick clock speeds. Along these lines, it can forcefully perform progressively fast tasks. All those activities incorporate increases, duplications, subtraction and so forth. Number of investigation is being performed on Vedic augmentation strategies. Investigation of power, size of chip and speed are the fundamental factor centered during the examination. Relative examination is likewise performed to feature the upsides and downsides of various methods to utilize Vedic increase in powerful way. To beat the engendering delay, the Vedic sutra that is Nikhilam is furthermore actualized in Vedic Multiplier. It diminishes the enormous number increase. Plan of Gabor channel dependent on Vedic science has likewise performed productive convolution.

Another strategy for amplification of marked number is offered in which Vedic multiplication is building block of its engineering. After extension of Vedic science, it is reached out to marked numbers utilizing the idea of RB number framework. It is clear that Vedic science application isn't constrained to whole number information

augmentation. The research can be further reach out to marked numbers. An efficient system for squaring activity is accounted for utilizing Vedic sutra without increase activity. A multiplier less squaring technique is being accounted for regarding rapid contrasting stall's multiplier and Vedic multiplier. The utilization of Vedic calculations, a period and zone productive circuit for factorial count is accounted. A different increasingly effective methodology for multiplier design is displayed when the sizes of both operands are the greater part of their most extreme qualities utilizing convey spare viper It is apparent that Vedic arithmetic is proficient adequate to pay key job in quick and solid calculation when contrasted with other traditional plans for increase.

- A. Multiplier Module of 2-bit contains 4 basic AND gates and half adders in 2 quantities. First including activity is performed. In stage-II expansion is finished. At last, connection is established. The engineering is being introduced in Figure 1.
- B. Vedic Multiplier: Our Multiplier's length is legitimately corresponding regarding emphasis, which thus prompts over the top equipment multifaceted nature, and which prompts huge power utilization and extreme deferral. In the above augmentation forms, just a single duplication process was done, all in all, the engendering postpones further increments. To beat these issues, the technique for parallel usage is considered in the proposed circuit execution, which successfully lessens multifaceted nature and increase steps.

3. URDHVA-TIRYAKABHYAM SUTRA

The multiplier relies upon the sutra "UrdhavaTiryakbhyam" of antiquated Indian ancient Vedic arithmetic. The sutra UrdhavaTiryakbhyam signifies "straight up and transversely".

It is a common duplication calculation that's appropriate to all kind of bit augmentation. The n*n bit number could be summed up by this sutra. The strategy utilized is of type structure that is accurate and syntactically and their all-out yield is acquired by adding the term in one single line utilizing UrdhavaTiryakbhyam sutra [8].

This parallel strategy is being utilized for getting the incomplete item and their totals. The clock recurrence is not being reliant on the multiplier. The upside of this is it lessens the need of microchip to work at high clock frequencies, which in turns builds preparing power.

By using Vedic multiplier, the processors creators can essentially stay away from the gadget calamitous disappointment. With the expanding

information and yield information transport width is since it has a significant standard structure, we can build the handling intensity of multiplier. The method utilized by this sutra, the circuit can be effectively executed on a chip of silicon.

"The benefit of this sutra is thought about when it is actualized for bits with higher number". The gate postponement and territory increment gradually as contrast with different multipliers for expanding in bits. Along these lines this calculation is demonstrated to be productive regarding force, reality.

[1] 2x2 bit Multiplier

For 2-bit Multiplication, we require 2-half adders and 4-AND gates. Multiplication process is defined by the following equations. [1]

$$\begin{aligned}
 s_0 &= a_0b_0 & (1) \\
 s_1 &= x_0 \text{ xor } x_1 & (2) \\
 s_2 &= x_3 \text{ xor } x_2 & (3) \\
 s_3 &= x_2 \text{ and } x_3 & (4)
 \end{aligned}$$

Multiplier 2x2 bit: The Vedic 2x2 bit multiplier's calculation is isolated into III stages. We are taking two numbers where each number has 2-bit. [2]. Now we are going to multiply these digits according to the function of each block. We use four basic AND-gates and two HALF-ADDER.

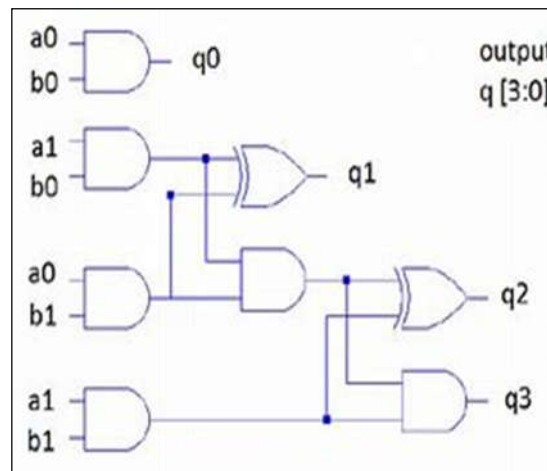


Figure. 1: 2-bit Vedic Multiplier [4]

[2] Multiplier 4 x 4bit:

A.4 -bit Multiplier: If we need of more bits at input. We have to differentiate the bit's number similarly into two isolates parts. How about we take 4-bit duplications, a3a2a1a0 and b3b2b1b0. The yield for the augmentation of 4-bit is composed as s7s6s5s4s3s2s1s0. Isolating the info bits in two sections, let say A3A2 and A1A0 for A and B3B2 and B1B0 for B. By utilizing the calculation of Vedic augmentation, for making 4-bit multiplier, we use 4-block of 2-bit multiplier and different

types of adder as shown in Fig.3. In Fig.2, the multiplication's basic structure is shown. [2]

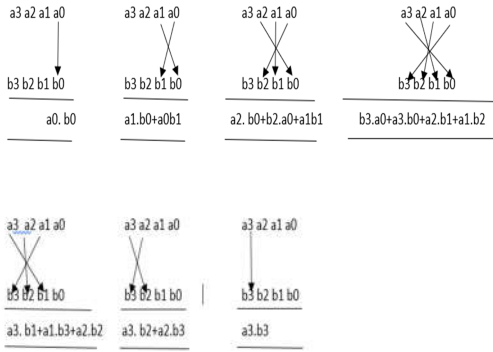


Figure 2 : 4-bit Vedic multiplier's functioning [6]

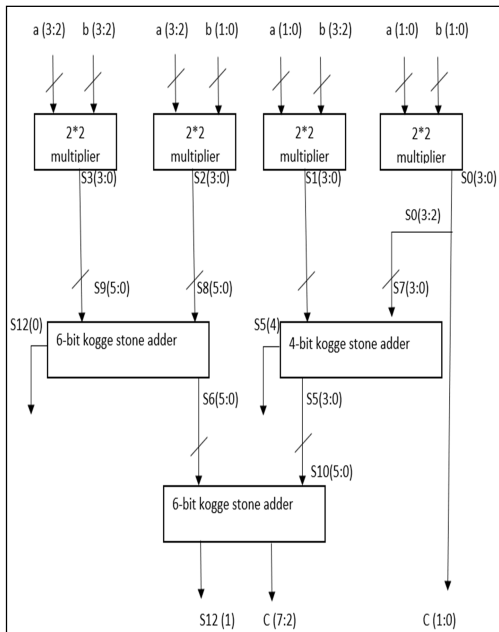


Figure.3: Vedic multiplier of 4x4 bit

4. 64X64 BIT MULTIPLIER

We can make 4-bit multiplier using 2x2 bit and 8-bit by using 4x4bit. Using 16-bit multiplier we can achieve 32x32 multiplier and using 32-bit multiplier we can get our proffered 64-bit multiplier. The recreation after effects of the considerable number of multipliers are being displayed in the further segments. By making 64 x 64 bit Vedic multiplier, we can see the result in some nanoseconds. It's block diagram is shown in Fig.4

We have used four 32-bit multiplier and three 68-bit kogge stone adder. Hence the values of the multiplier can be get from the above diagram.

Here value of S5(67:0), S6(67:0), S8(67:0), S10(67:0) and S11(67:0) can be find out using this method.

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S5(67: 0) <= ('0' & S3(66: 0));
S6(67 :0) <= ('0' & S2(66 :0));
S8(67:0) <=
("00000000000000000000000000000000" &
 S1(66: 32));
S10(67: 0) <=
("00000000000000000000000000000000" & S7(68)
 & S9(67: 32));
S11(67: 0) <= ('0' & S4(66: 0));
    
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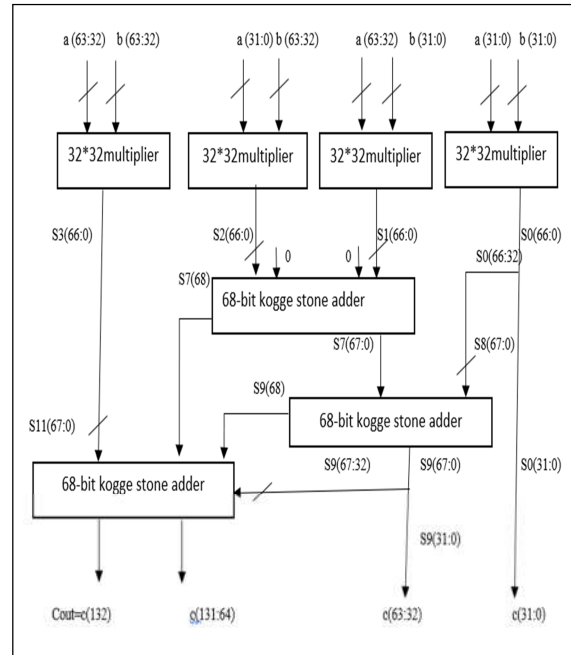


Figure.4: Schematic of 64*64 bit multiplier

In this paper we are using KOGGE STONE ADDER in spite of RIPPLE CARRY ADDER.

5. KOGGE-STONE ADDER

Carry Look-ahead Adder's advance version is Kogge-stone adder . During implementation Kogge-Stone adder consumes more area with respect to other adders , it has paralld prefix. So the carry is generated and transferred paralldly. It is the fastest adder with based on designing time. It is mostly use adders in industry. Harold S. Stone and Peter M. Kogge introduced to the world with the first Kogge-Stone Adder in 1973. The building block of 4-bit Adder presented by Kogge & Stone is shown below.[10]

Parallel Prefix Adders essentially comprises of 3 phases. [11]

1. Stag1-I Before -processing
2. Stage-II Process of Carry generation
3. Stage-III After-Processing

1. BEFORE -PROCESSING

pi = Ai xor Bi(4)
 gi = Ai and Bi(5)

2. PROCESS OF CARRY GENERATION

$$P_{m:n} = P_{m:k} \text{ and } P_{k-1:n} \dots\dots\dots(6)$$

$$G_{m:n} = G_{m:k} \text{ or } (P_{m:k} \text{ and } G_{k-1:n}) \dots\dots(7)$$

Black/grey cells implement the given two equations, which will be usually used in the following discussion on prefix trees.[11]

3. AFTER-PROCESSING

It is used to compute the sum bits. The logic equation of the sum bit signals is given below. [11]

$$S_i = P_i \text{ xor } C_{i-1} \dots\dots (8)$$

A. Carry equation of kogge stone adder[3]

$$C_0 = G_0.P_0 \dots\dots\dots(9)$$

$$C_1 = (P_1.G_0 + G_1) + P_1.P_0 \dots\dots\dots(10)$$

$$C_2 = P_2.P_1.(G_0 + P_0) + (P_2.G_1 + G_2) \dots\dots\dots(11)$$

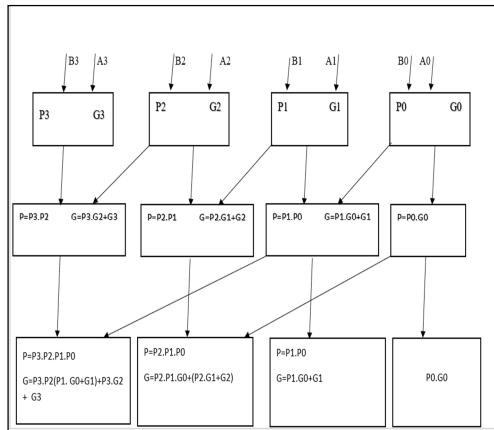
$$C_3 = P_3.P_2.C_1 + (P_3.G_2 + G_3) + P_3.P_2.P_1.P_0 \dots\dots\dots(12)$$

B. Sum equation of kogge stone adder[3]

$$S_0 = P_0 \dots\dots\dots(13)$$

$$S_1 = P_1 \text{ XOR } C_0 \dots\dots\dots(14)$$

$$S_2 = P_2 \text{ XOR } C_1 \dots\dots\dots(15)$$



$$S_3 = P_3 \text{ XOR } C_2 \dots\dots\dots(16)$$

Figure.5: 4-bit Kogge-stone adder's block diagram [3]

6. EXPLORATORY YIELD

The reenactment of proffered 64-bit multiplier has been done to ascertain the most minimal Way postponement for various multipliers. this segment additionally incorporates the comparative outcome investigation of Vedic propagator and recently structured enlarger. The table-1 represents the region use of proffered Vedic multiplier.

Table 1: Device Utilization Summary of 64-Bit Multiplier

	Logic Utilization		
	USED	AVAILABLE	UTILIZATION
Count of slice LUT's	10313	63400	16%
Count of completely used LUTs-ff pairs	0	10313	0%
Number of bonded IOB's	261	210	124%

Moreover, to demonstrate the effectiveness of our proffered Vedic arithmetic dependent 64-multiplier, the integrated report and reproduction output is being contrasted and the presently structured 64-bit multiplier utilizing an equivalent calculation. We have utilized ripple carry adder already is contrasted and the 64-bit multiplier utilizing kogge stone adder.

Multiplier Using	DELAY(NS)			
	8 Bit	16 Bit	32Bit	64 Bit
Ripple Carry Adder	9.097	17.917	36.006	70.107
Kogge Stone Adder	8.467	15.831	34.693	66.276

7. RESULTS

A.64-bit Vedic multiplier

1)RTL view

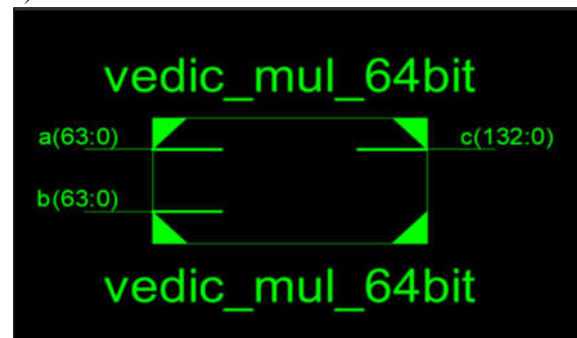


Figure 6: 64-bit Vedic multiplier's RTL view

Figure 6 shows the RTL view of 64-bit Vedic Multiplier. It shows the register transfer logic view of the Unit. It consists of Vedic multiplier and KSA adder.

2) Detailed RTL view of 64-bit multiplier:

Figure 7 shows the RTL view of 64-bit Vedic Multiplier. It shows the register transfer logic view of the Unit. It consists of Vedic multiplier and KSA adder.

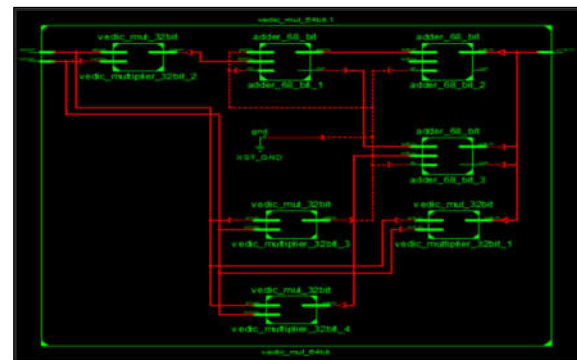


Figure.7: 64-bit multiplier's detailed view

